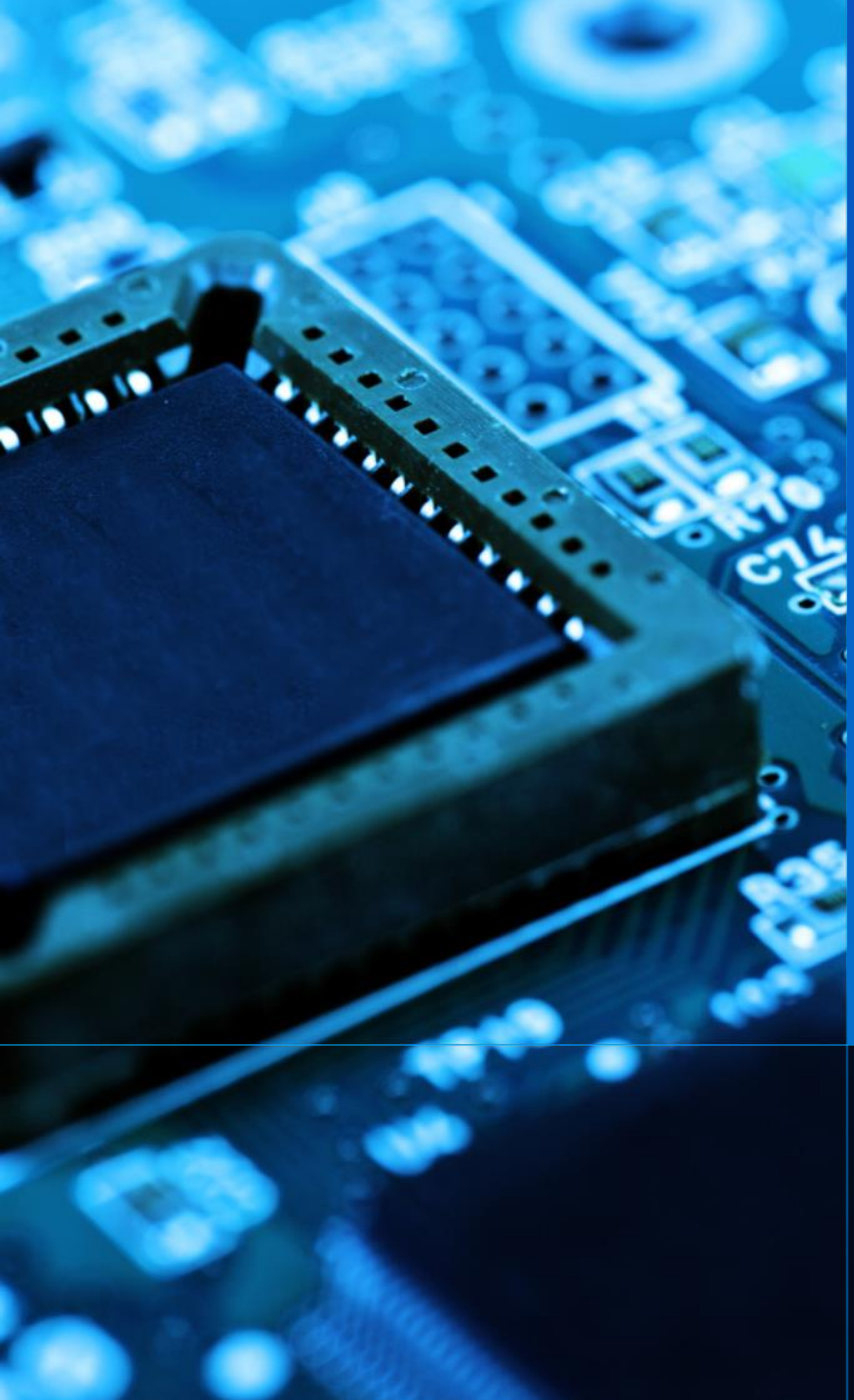


ASML

E-Beam Inspection and Metrology: Developments and Applications in Lithography

Yu Cao

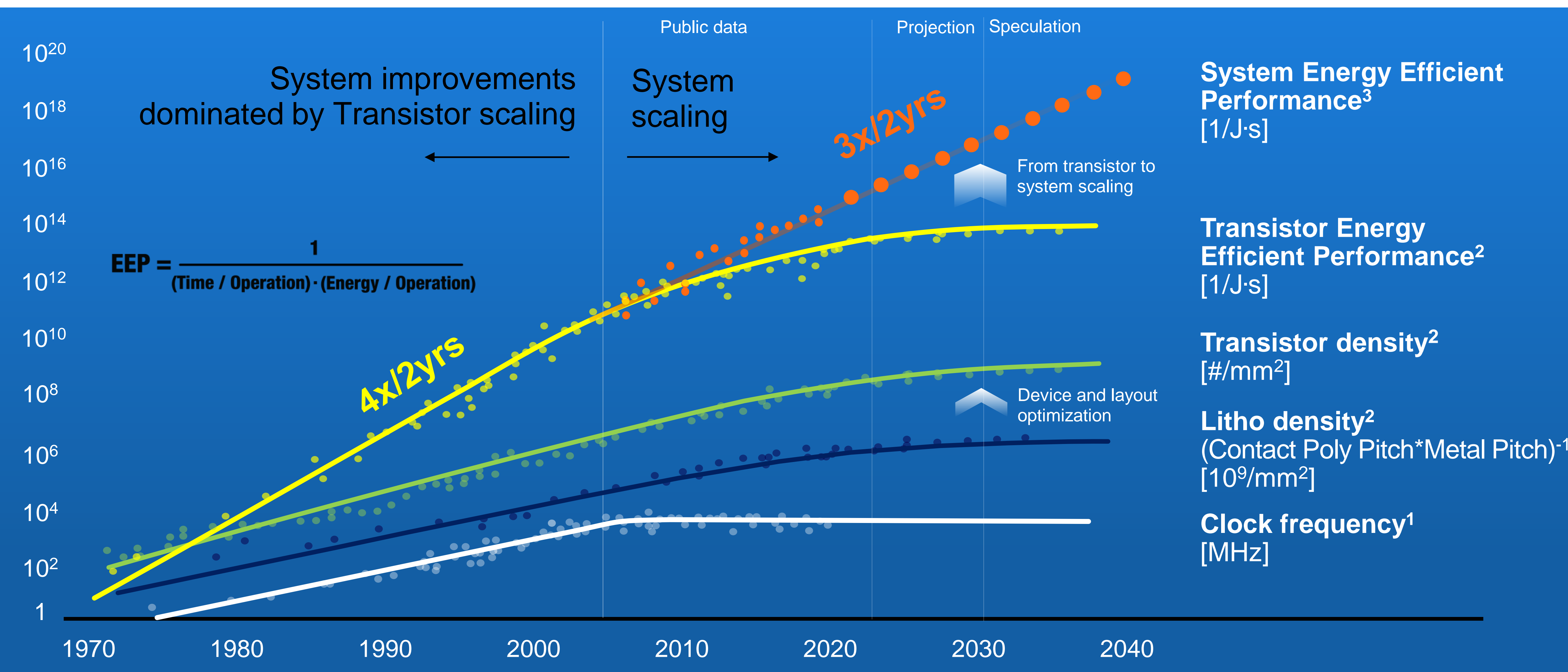
Hermes Microvision, Inc., an ASML company

February 28, 2023
San Jose, California

V1

Moore’s Law evolution: The next two decades

From cost per transistor through density, to cost of time and energy through systems



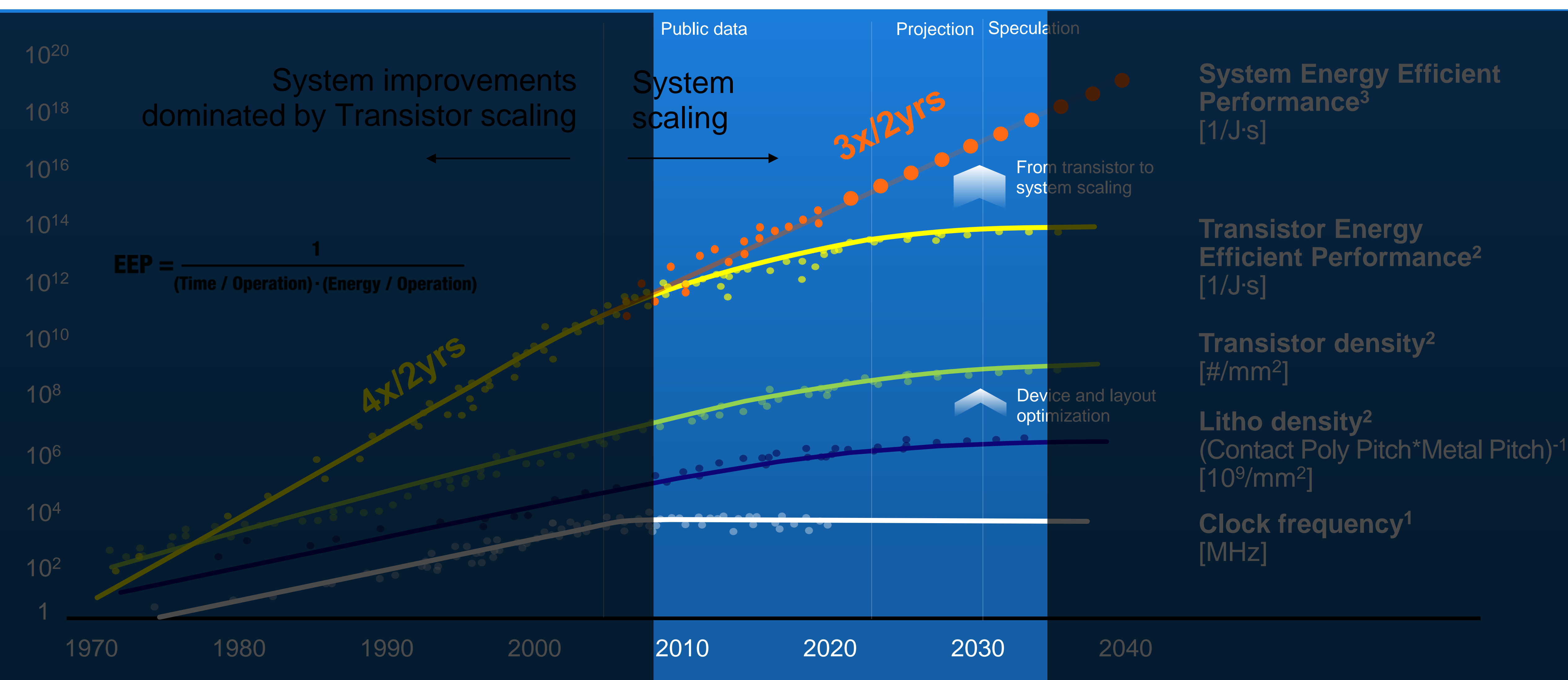
ASML

Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

Public

Moore’s Law evolution: The next two decades

From cost per transistor through density, to cost of time and energy through systems

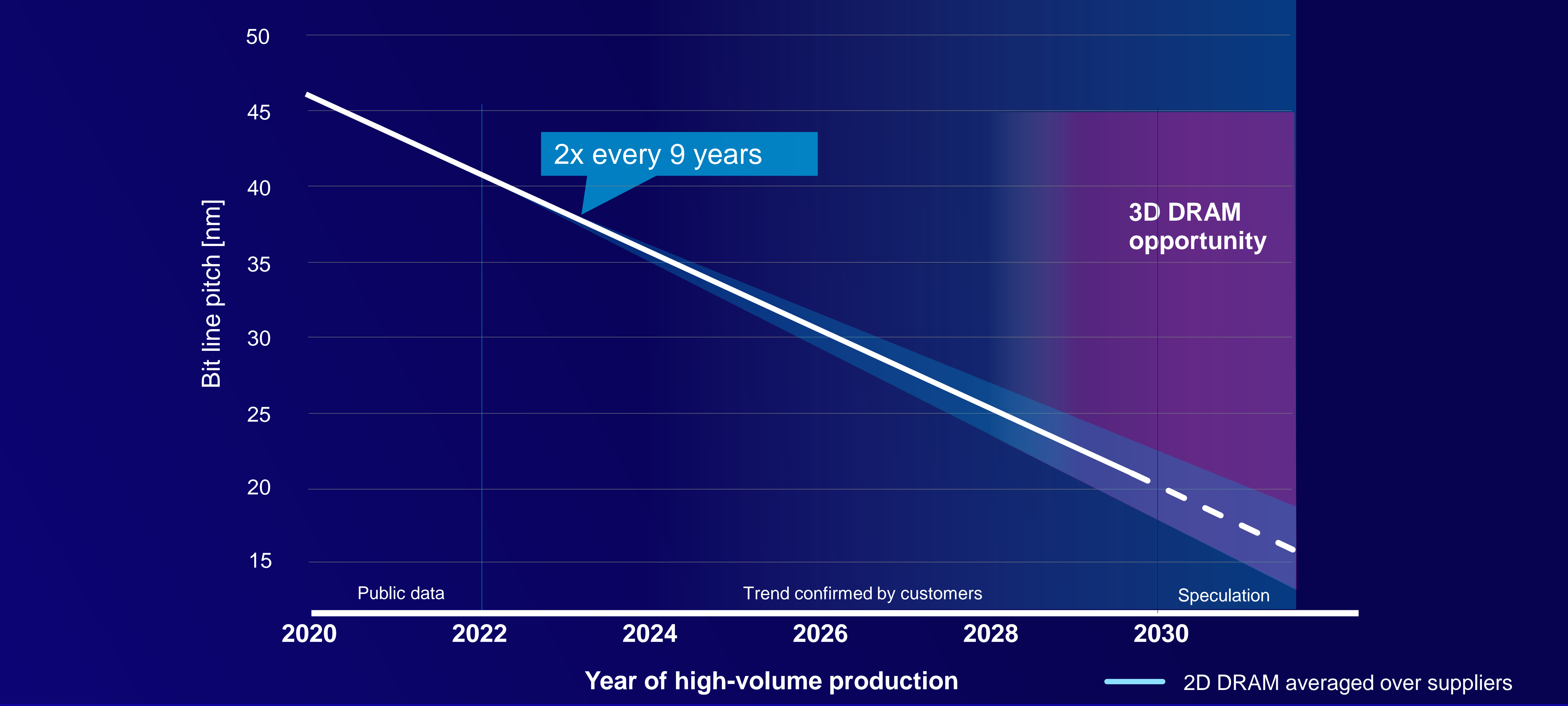


ASML

Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

Public

Trend 1: Litho density scaling continues (e.g., coming decade for DRAM), driving need for resolution in inspection & metrology

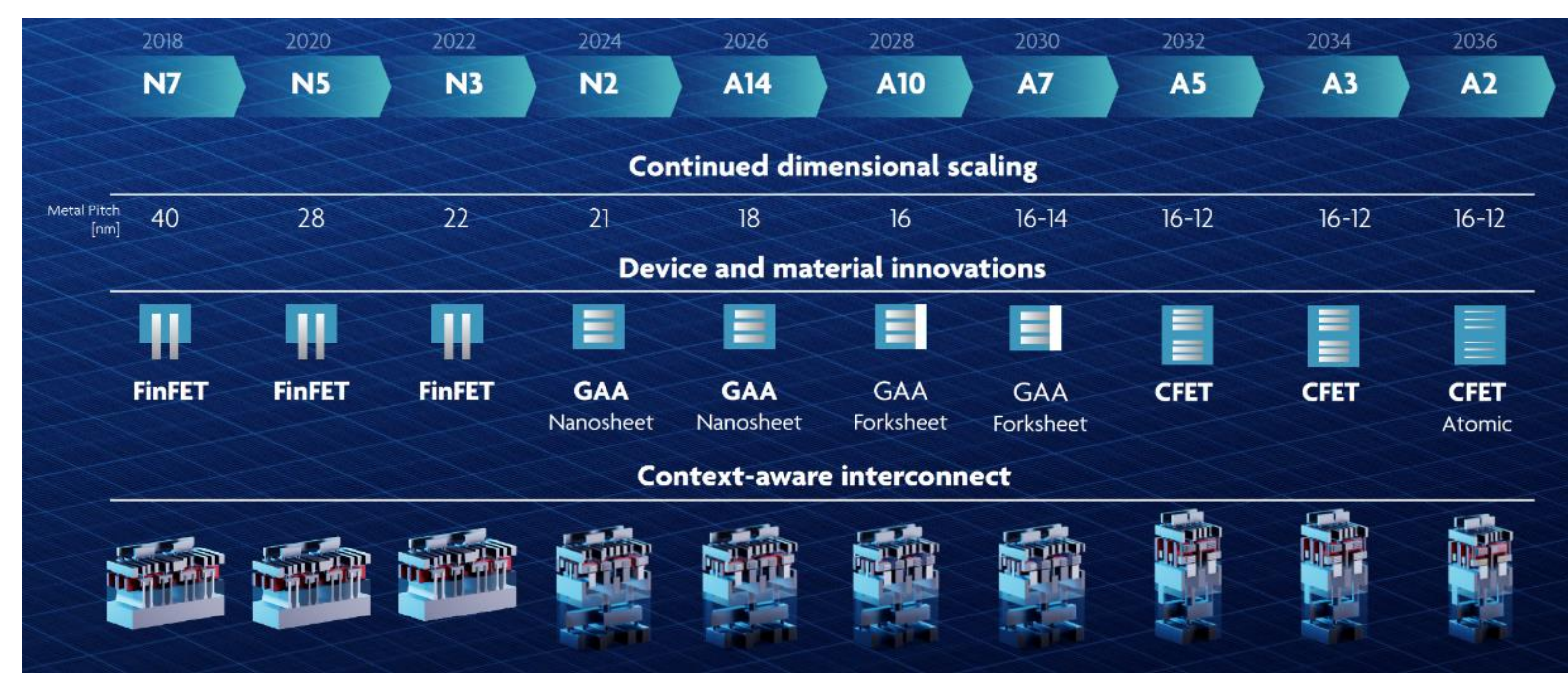


ASML

Source: Average customer roadmap extended by ASML extrapolation May 2021, averaged with the International Roadmap for Devices and Systems 2021.

Public

Trend 2: Increasing use of 2.5 & 3D scaling drives need for high aspect ratio & buried feature inspection & metrology



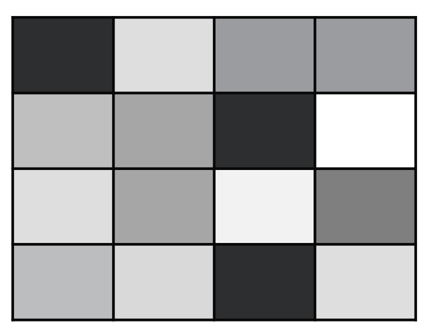
Source: Luc van den Hove, IMEC. “The endless progression of Moore’s Law” ISS, April 2022

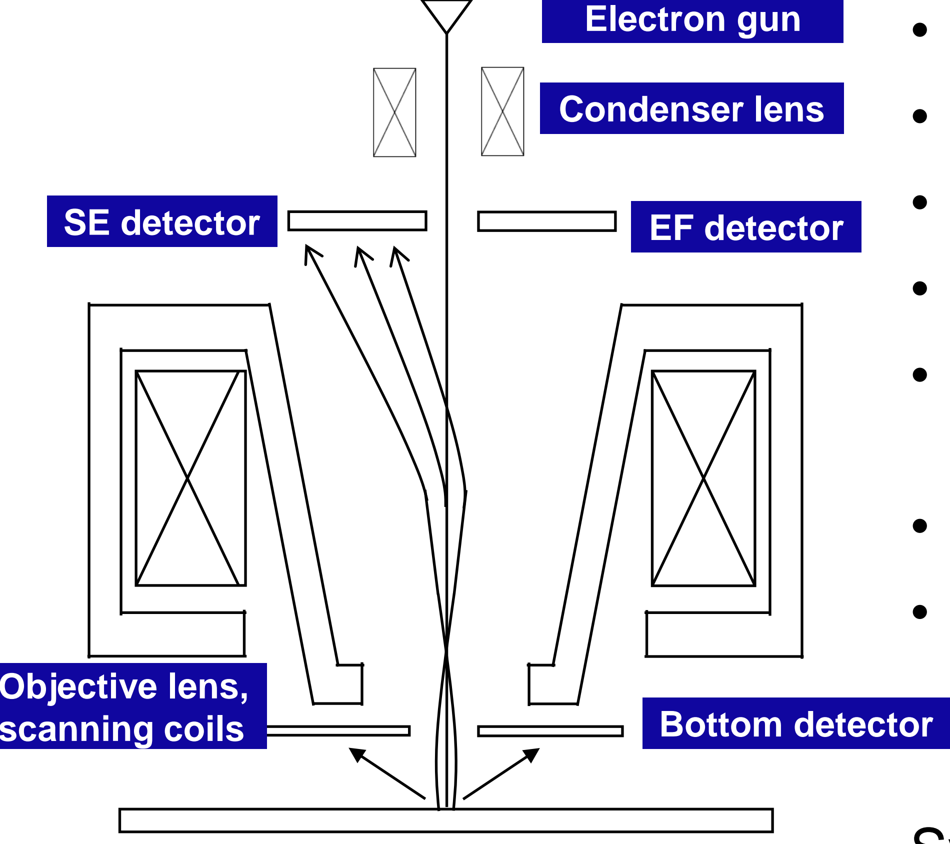
2F
2F
Vp
storage cap.
VCAT
BLi+1
BLi
BLi-1
WLi-1 WLi WLi+1
P-sub.

Source: KW Song et al.- A VCAT-based 4F2 DRAM, IEEE 2009

SEM Components

Gray level image on display





Operation

- **Electron gun** emits beam of electrons
- **Anode** accelerates electrons
- **Condenser lens** collimates the beam
- **Objective Lens** focuses beam onto sample
- **Deflectors-Scanning Coils** raster scan the focused beam over sample
- **Detectors** collect emitted signal from sample
- **Image Display system** synchronizes signal with scan position to form image.

System requirements

- High vacuum – allow electrons to travel unimpeded
- High voltage - draw electrons from source and accelerate down the column

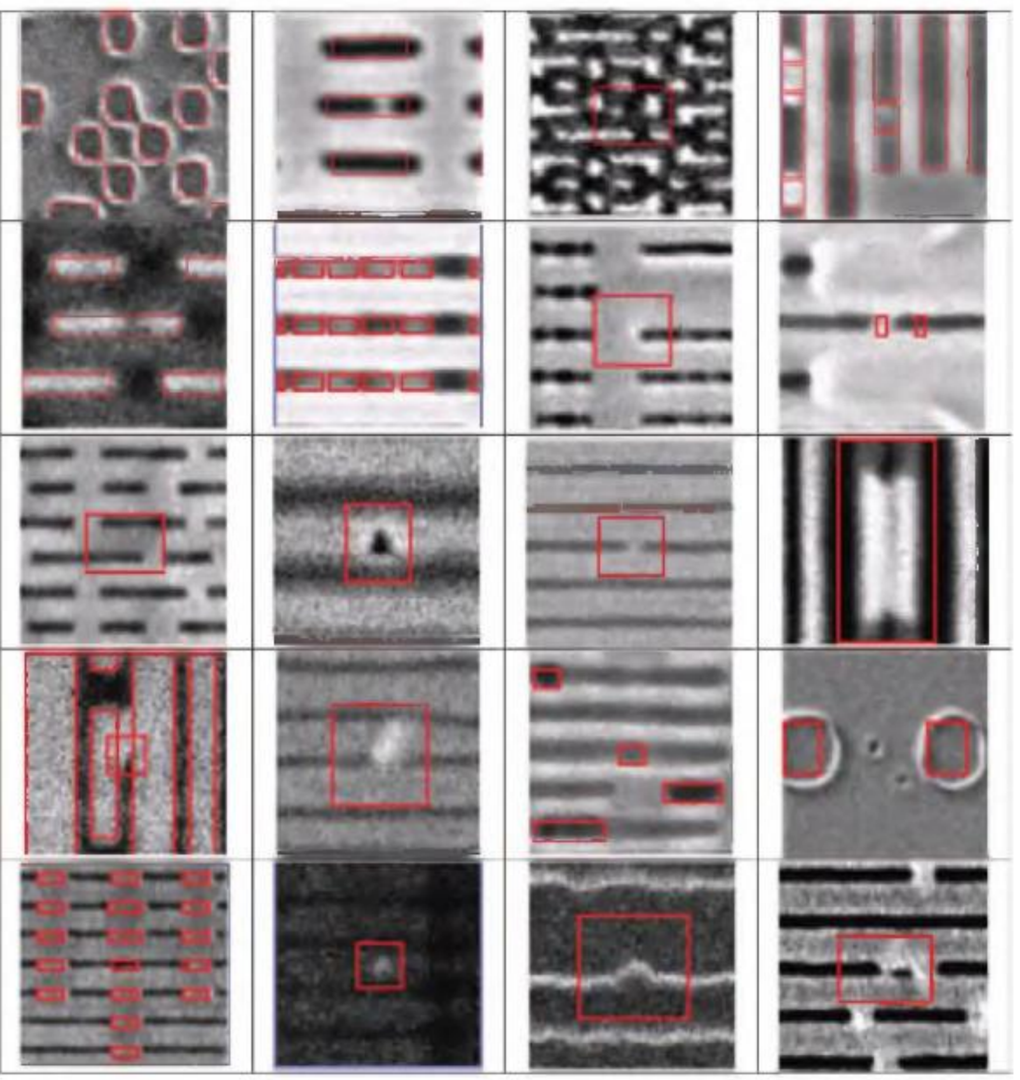
Public

ASML operates in 3 main e-beam categories: metrology, voltage contrast defect inspection, and physical defect inspection

Using SE (secondary electron) and BSE (back-scattered electron) to form images for inspection/metrology purpose

Application	Metrology	Inspection	
Category	CD, EPE, and OVL metrology	Voltage Contrast electrical defect inspection	Physical defect inspection
Example			
Description	• CD/EPE measurement • OVL measurement / OVL margin estimation	• Logic devices: Gate/Contact/BEOL • DRAM devices: Contact for cell & periphery • 3DNAND devices: Channel hole/contact	• Physical defects in nm scale beyond optical tool resolution

Why does the industry need e-beam inspection?



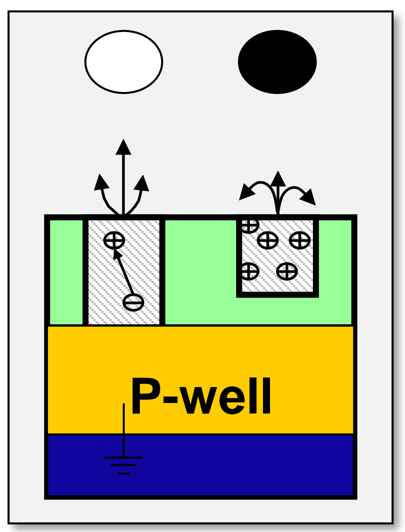
A gallery depicting critical defects of interest detected using the electron beam inspection system mentioned in this chapter. Note that none of these defects were originally detected by any optical inspection tool, regardless of inspection time.

Tuyen Tran, Metrology and Diagnostic Techniques for Nanoelectronics, 1st edition, 2016, ISBN-10: 9814745081

However, e-beam inspection throughput limits HVM applications except in 3DNAND

E-beam voltage contrast inspection is the only viable solution for electrical defect detection

Voltage contrast inspection relies on the build-up of surface potential difference exerting field to influence the trajectories of secondary electrons

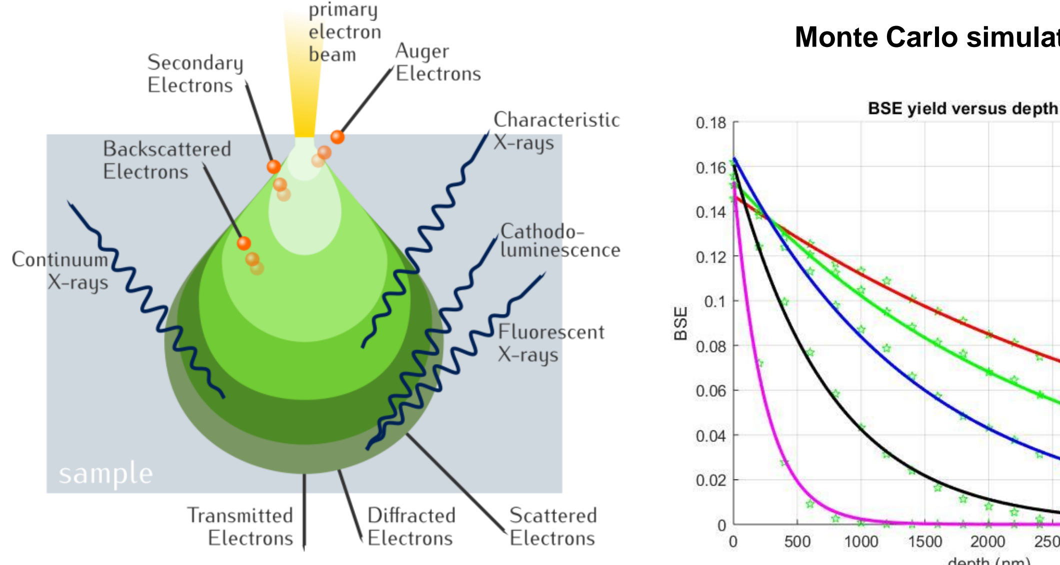


Voltage Contrast Model

	DRAM	3D NAND
Top view EBI image		
Cross-section View		
Failure Mechanism	*Thin nitride remain at bottom of storage node contact*	*dielectric remain at bottom of memory channel hole*

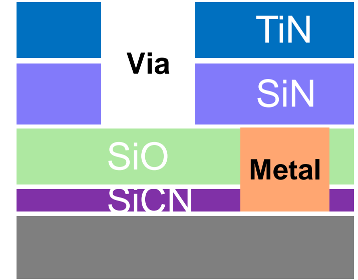
E-beam is capable of inspecting physical defects both on wafer surface and buried in 3D structures at high resolution over a wide landing energy range

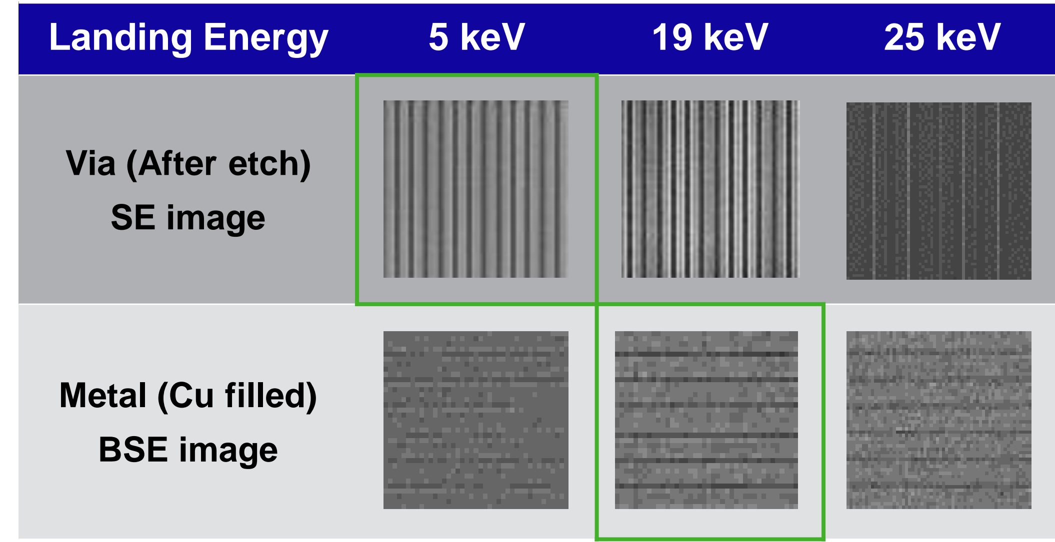
- Secondary electrons have very low energies on the order of 50 eV → shallow depth (~ a few nm), high resolution
- Back scattered electrons are reflected from the sample by elastic scattering, and have much higher energy → large penetration depth (up to a few micron), low yield



https://en.wikipedia.org/wiki/Scanning_electron_microscope

- HMI supports high throughput secondary electron (SE) and back scattered electron (BSE) inspection with multiple detectors (in-lens and bottom detectors)
- Landing energy optimized for different penetration depth



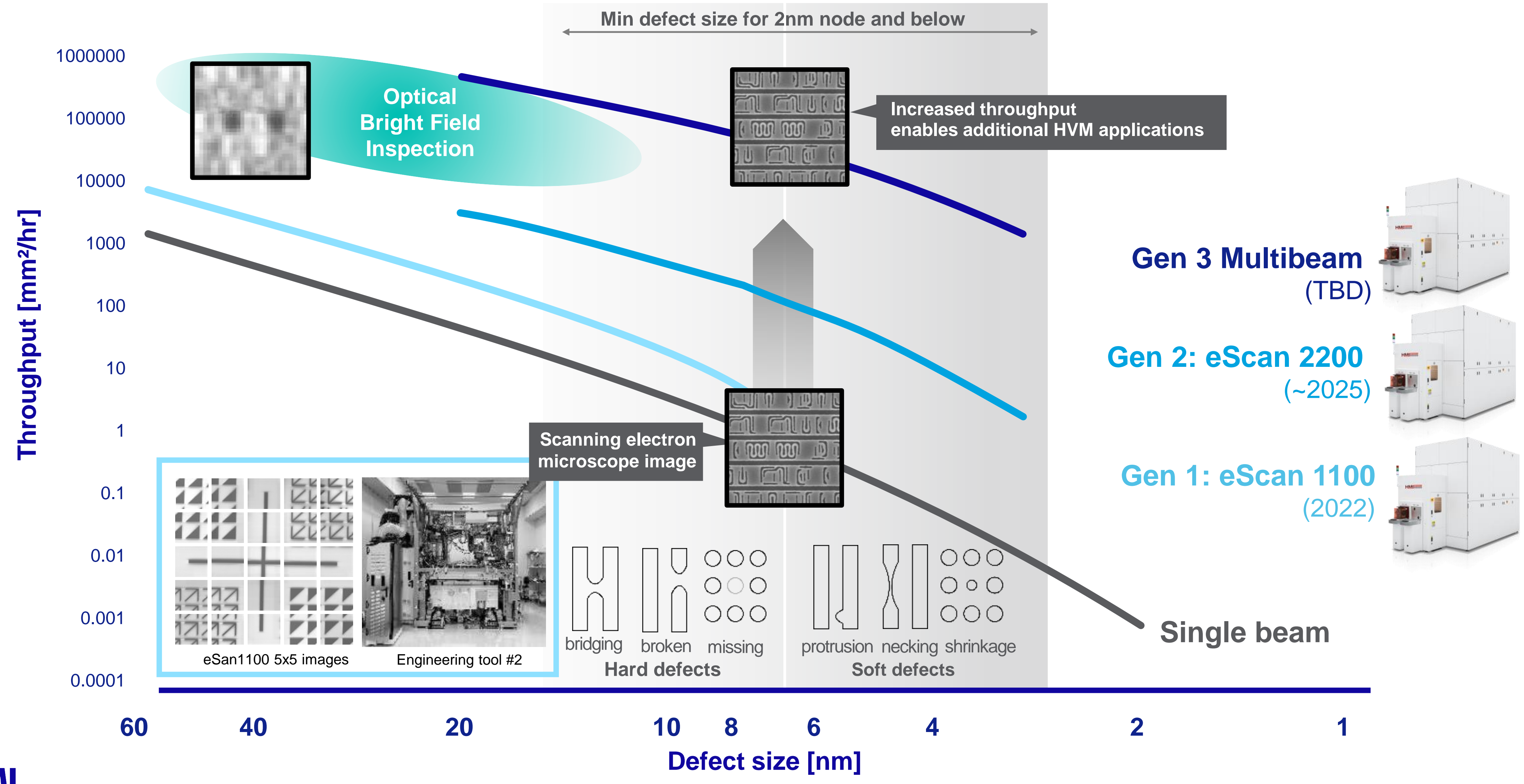


Landing Energy	5 keV	19 keV	25 keV
Via (After etch) SE image			
Metal (Cu filled) BSE image			

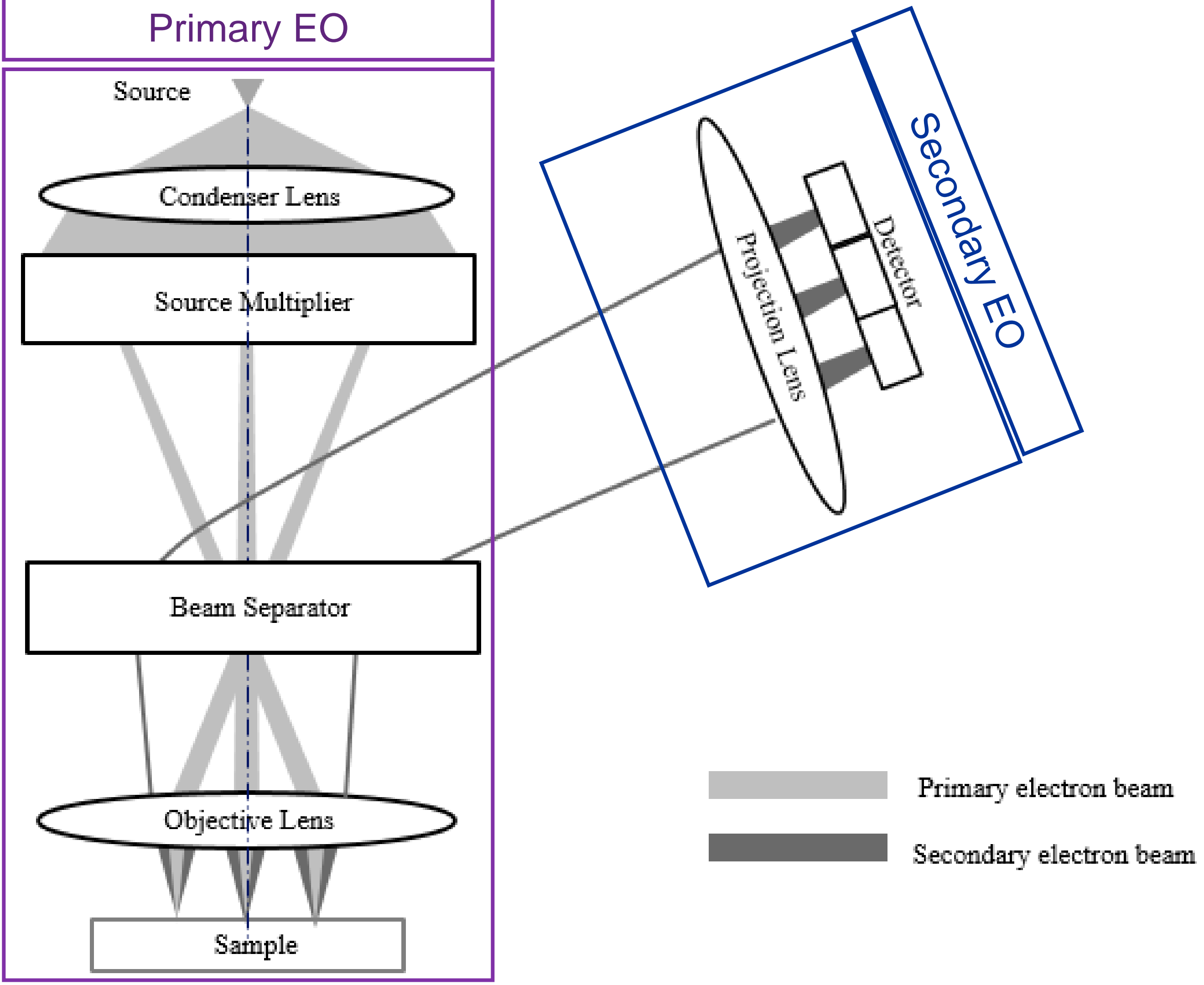
Public

E-beam inspection has inherent resolution advantage

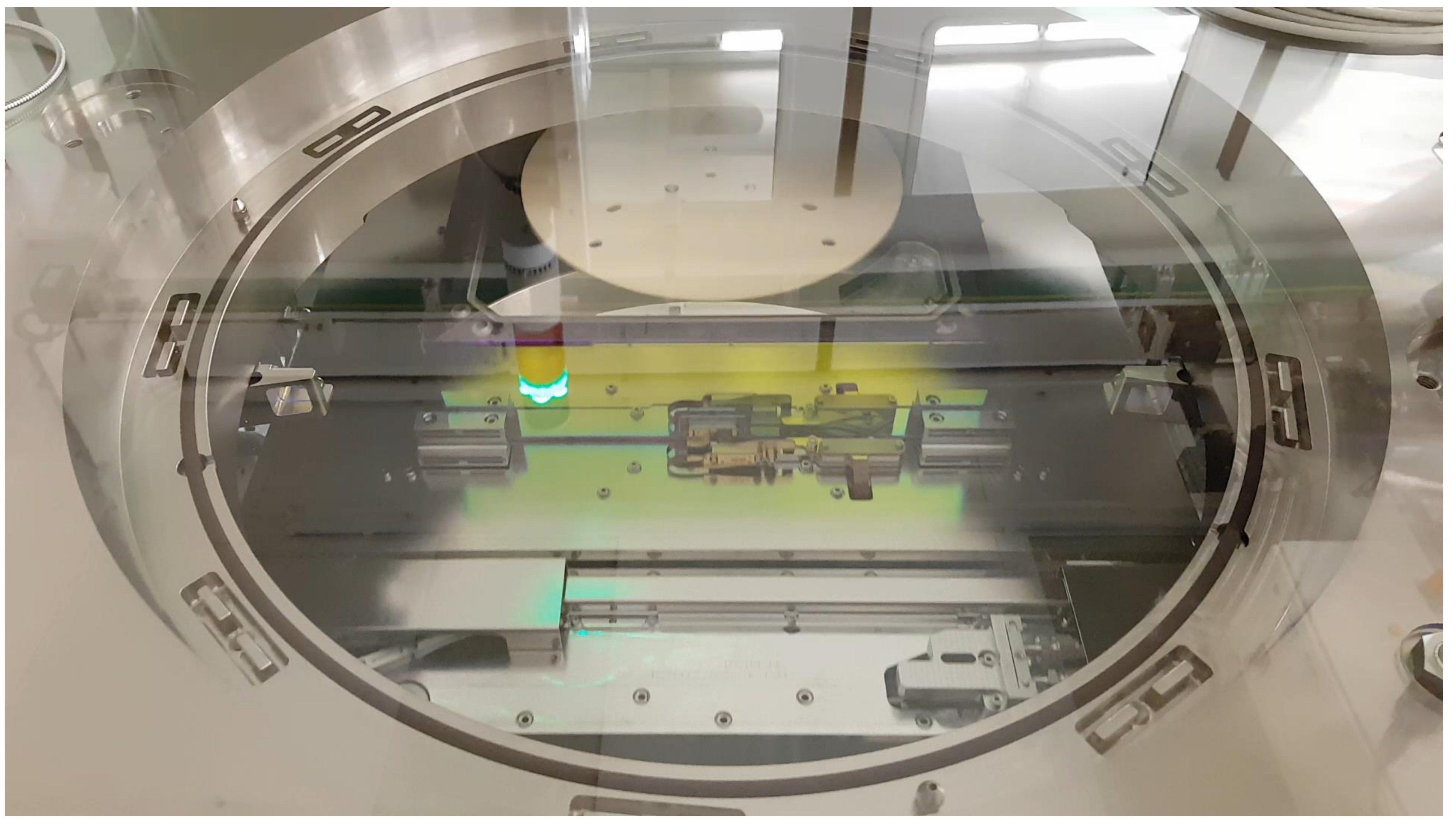
Increasing throughput through increasing parallelism with multibeam



HMI's multibeam electron optics design

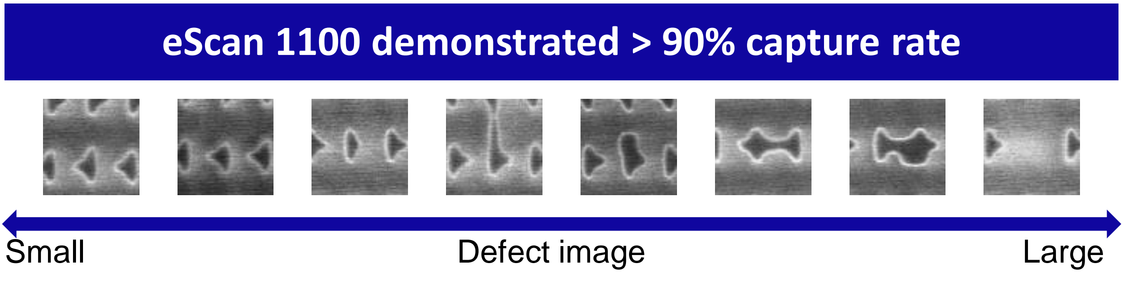


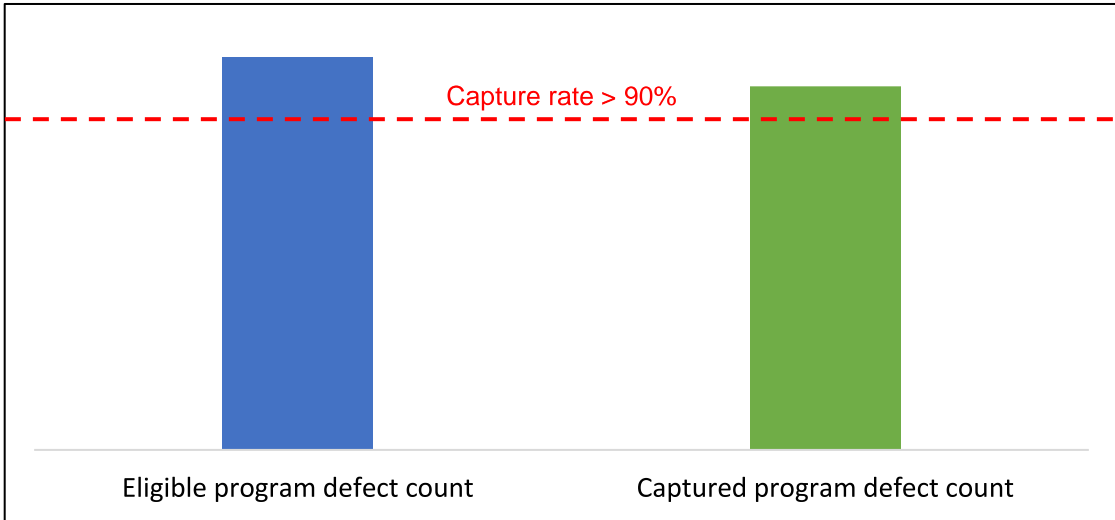
High-speed wafer stage designed in Veldhoven



eScan 1100 (5x5 multibeam): > 90% capture rate and consistent performance among all 25 beams

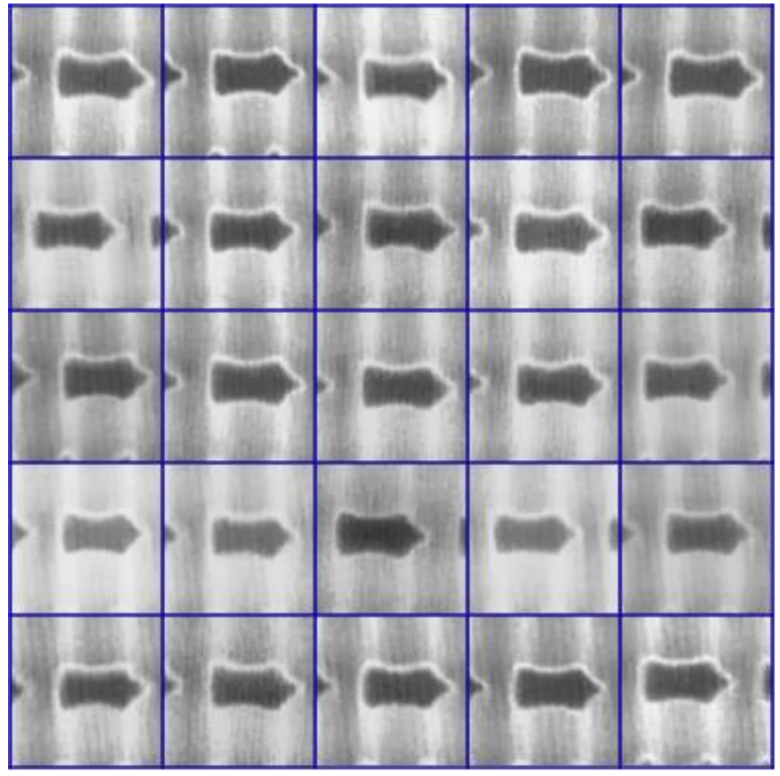
eScan 1100 demonstrated > 90% capture rate





Verification based on programmed defects on HMI test wafer

25 beams show consistent results

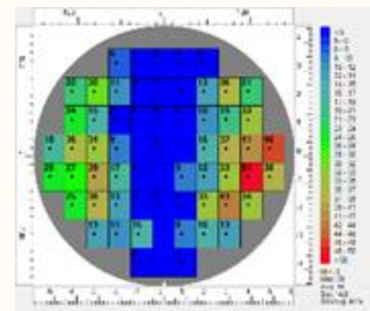


Images from the same programmed defect through 25 beams

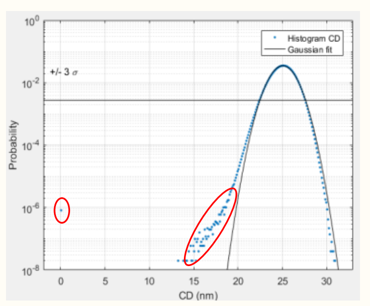
eP5 enables massive metrology applications

eP5 capabilities
High resolution @ 1 nm ▪ Sensitivity: 0.05 nm ▪ Precision: < 0.1 nm
Large field-of-view (FOV): 12k pixel scan width for metrology and inspection
Design-based metrology for Process Window, OPC and EPE applications
High speed: 5~30x throughput vs. conventional CD-SEM metrology

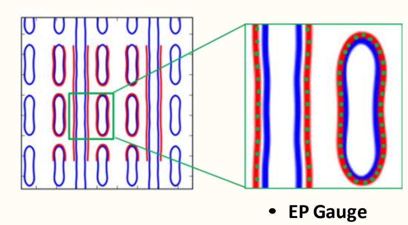
1. High resolution defect metrology



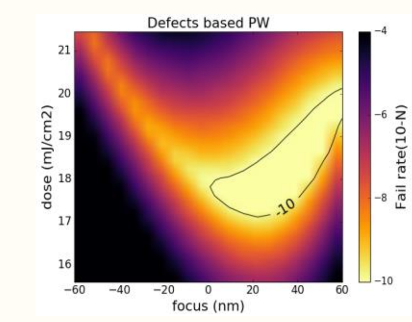
2. Massive CD metrology



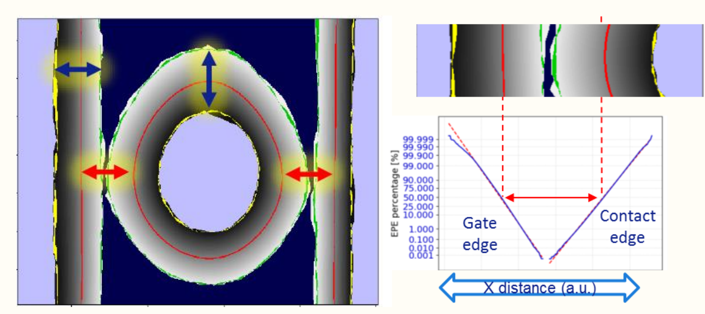
3. Massive OPC metrology



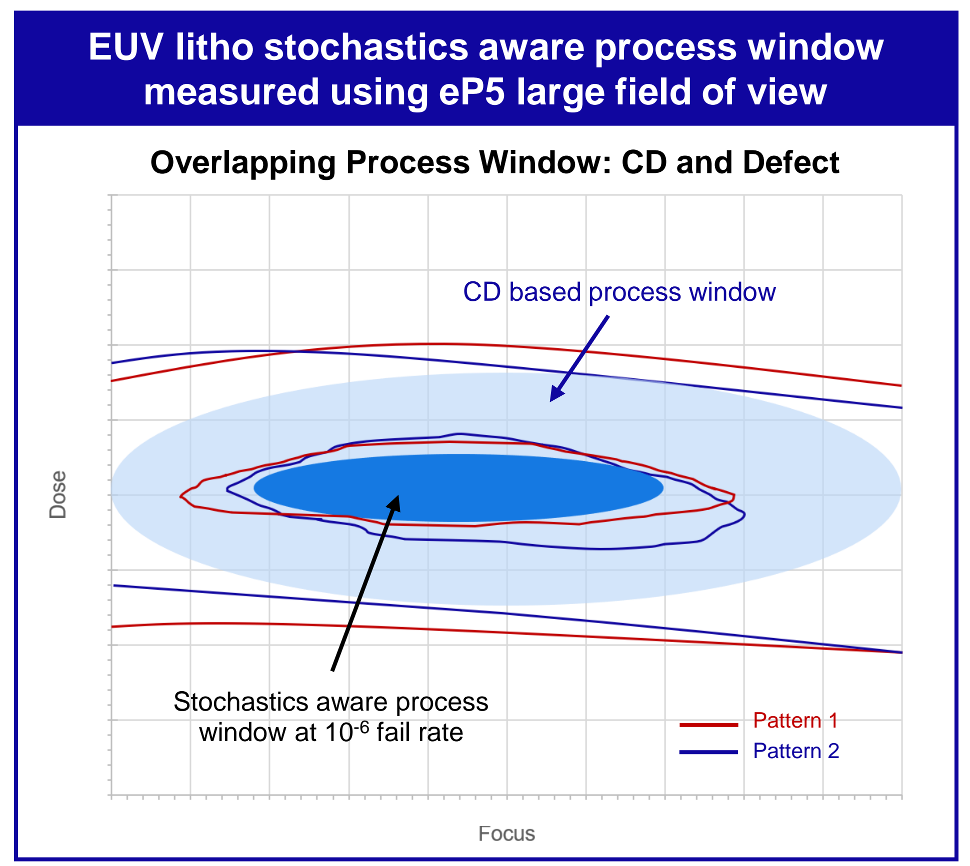
4. Stochastics aware process window metrology

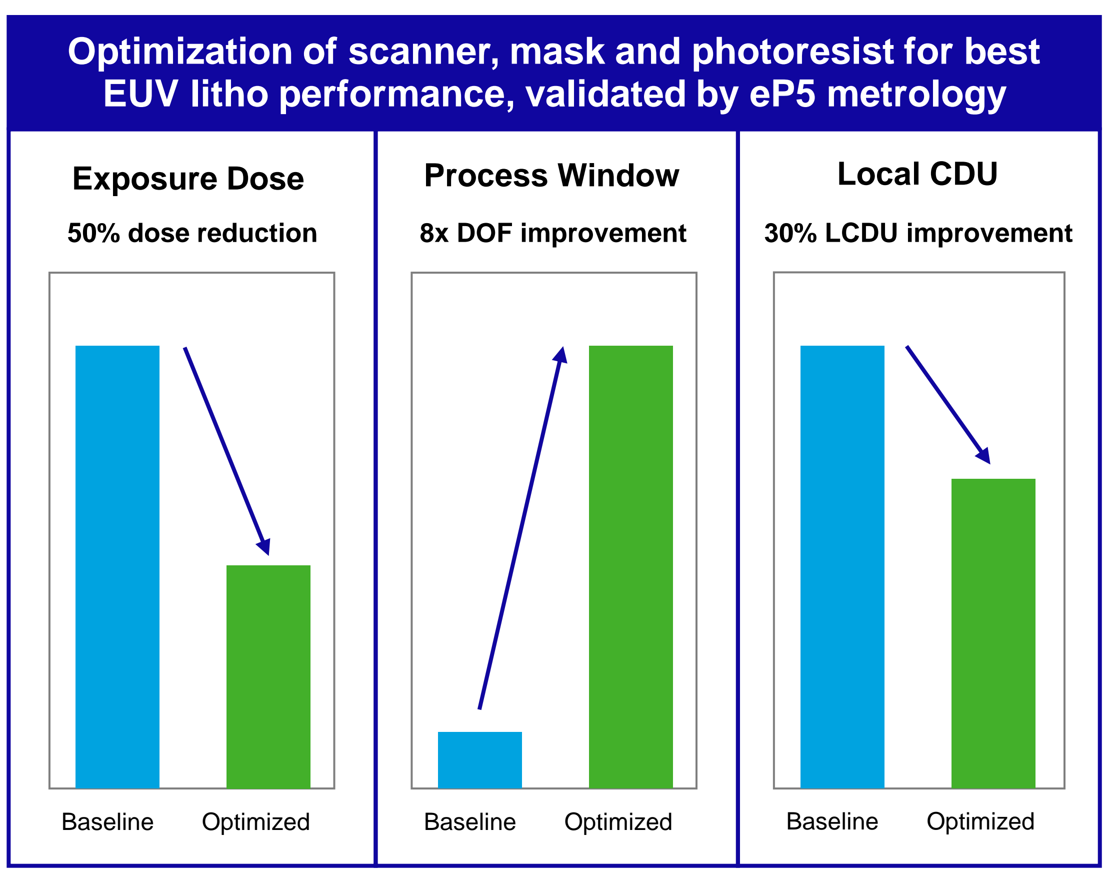


5. Edge placement error metrology



Collaboration with Micron in EUV lithography optimization to mitigate stochastic effects using eP5 large field of view metrology





- CD based process window misses the stochastic pattern defects, overestimating the process window
- eP5 Process Window Metrology identified scanner and mask optimizations and facilitated resist screening, critical for **maximizing EUV scanner productivity of good yielding dies**

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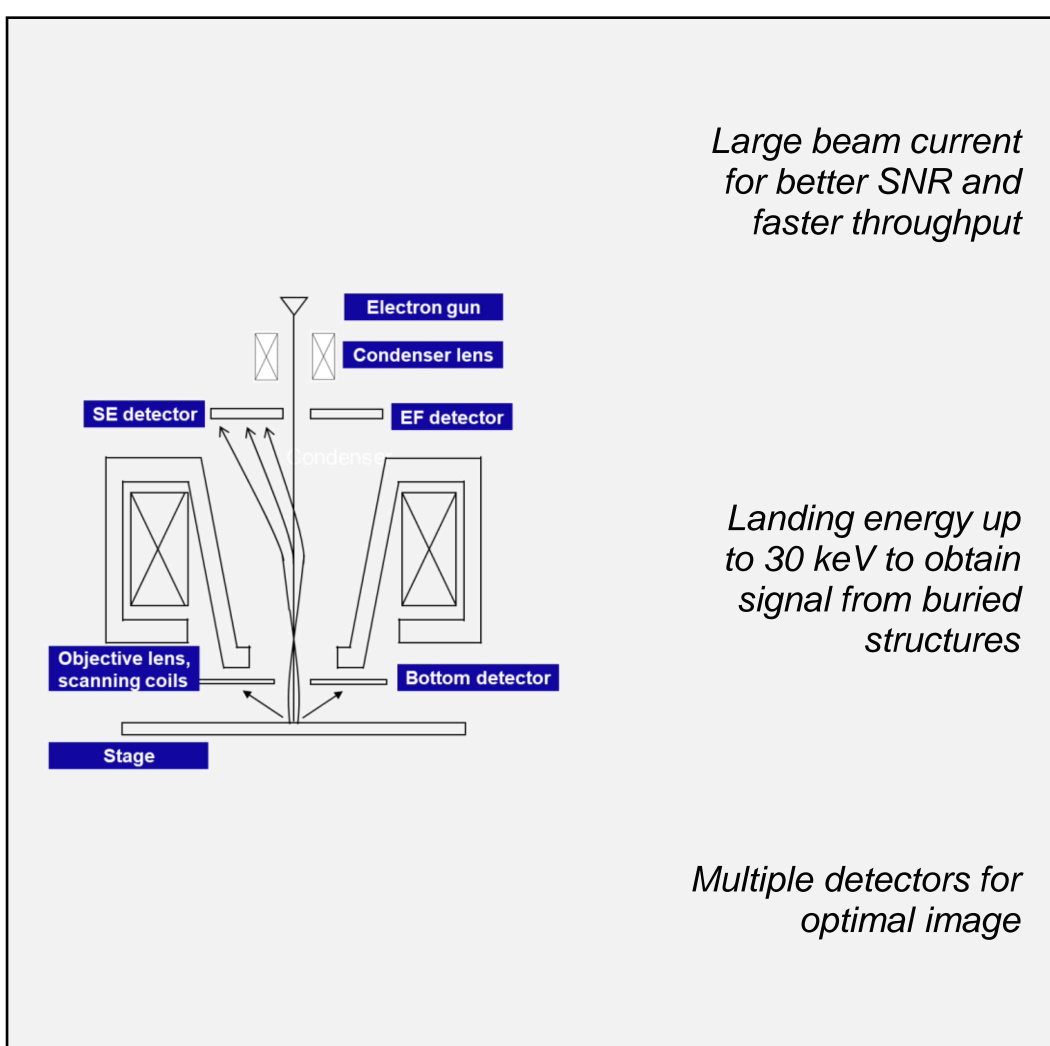
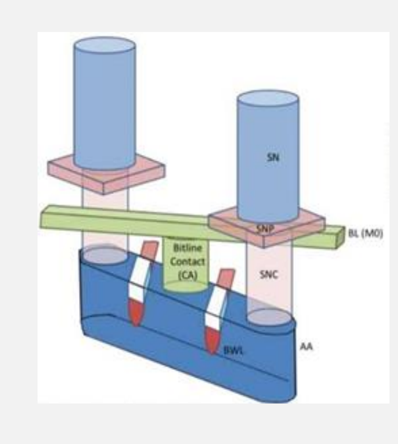
Public

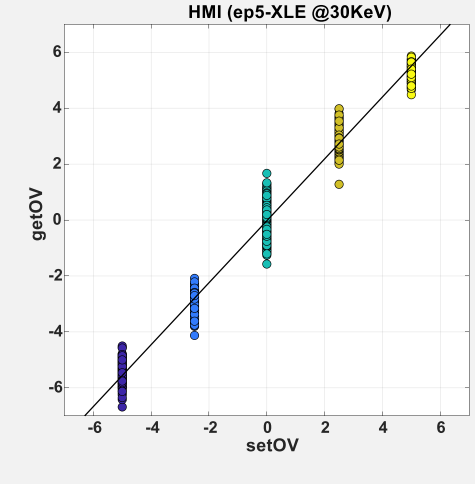
ePSXLE: High Accuracy in-device Overlay Measurements at Speed



- HMI eP5 XLE supports high throughput metrology and inspection using secondary electron (SE) and back scattered electron (BSE) with multiple detectors
- Landing energy optimized for different penetration depth for best performance

Set-Get validation of eP5 XLE overlay metrology accuracy: DRAM Bit Lne to Active overlay after etch, 30 keV)





Public

What does Edge Placement Error (EPE) budget look like?

EPE budget is dominated by local errors, followed by overlay and OPC

Local placement errors

Global overlay errors

Global CD errors

local CD and placement errors

global overlay error

Global CDU

OPC

Local CD errors

Line edge roughness

OPC errors

Via

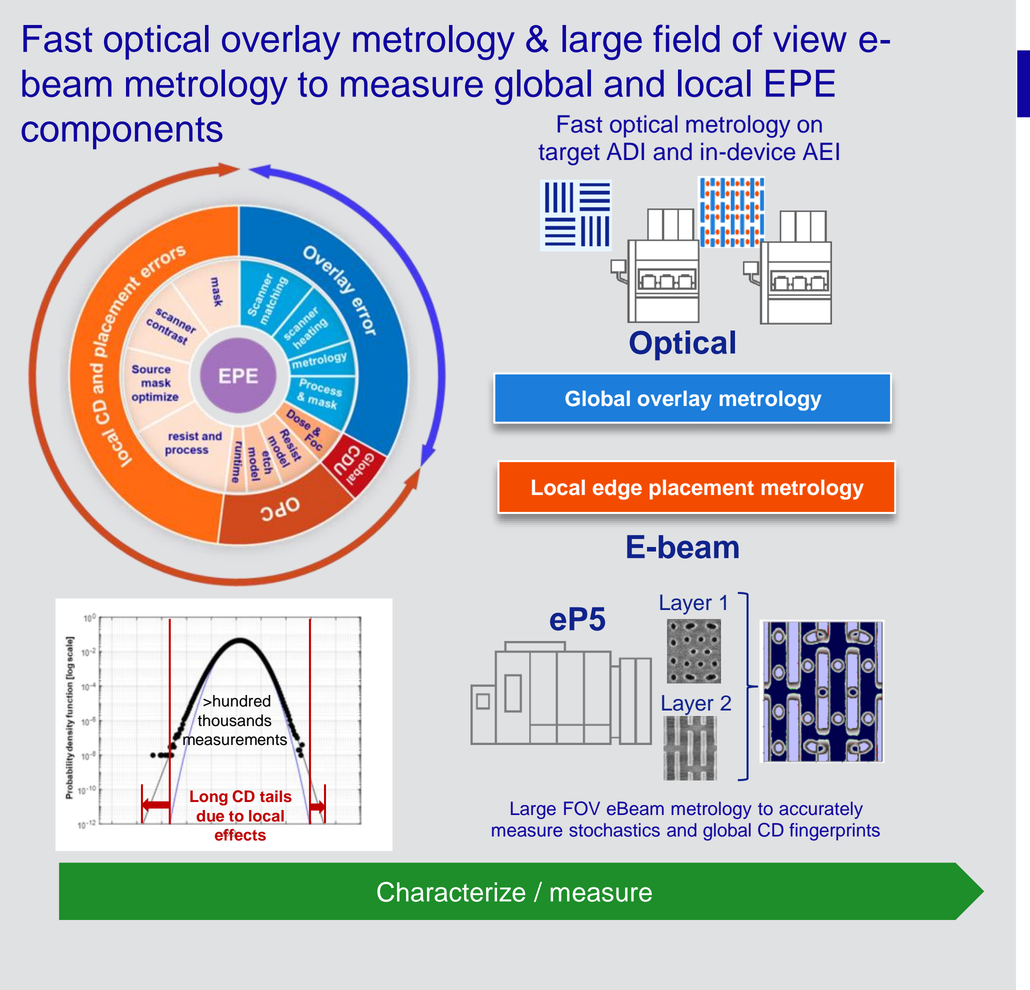
Metal

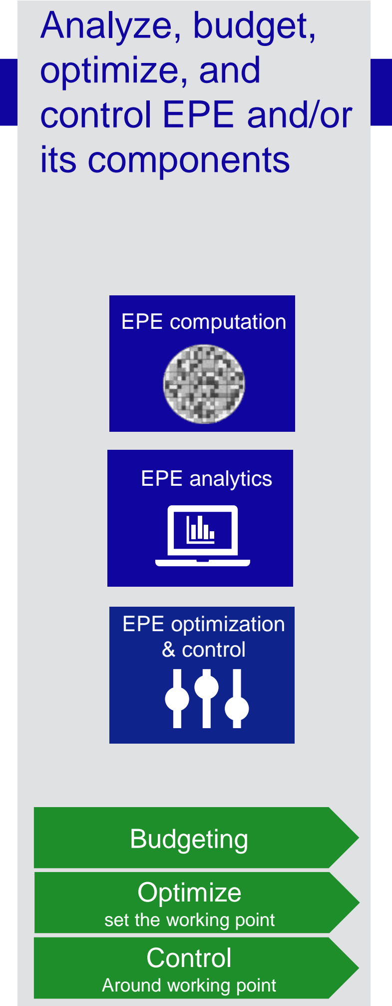
Edge **P**lacement **E**rror (EPE) budget for EUV N5 IMEC logic case, combining errors of overlay & CD uniformity (global CDU, local CD, placement and OPC errors) for combined layers

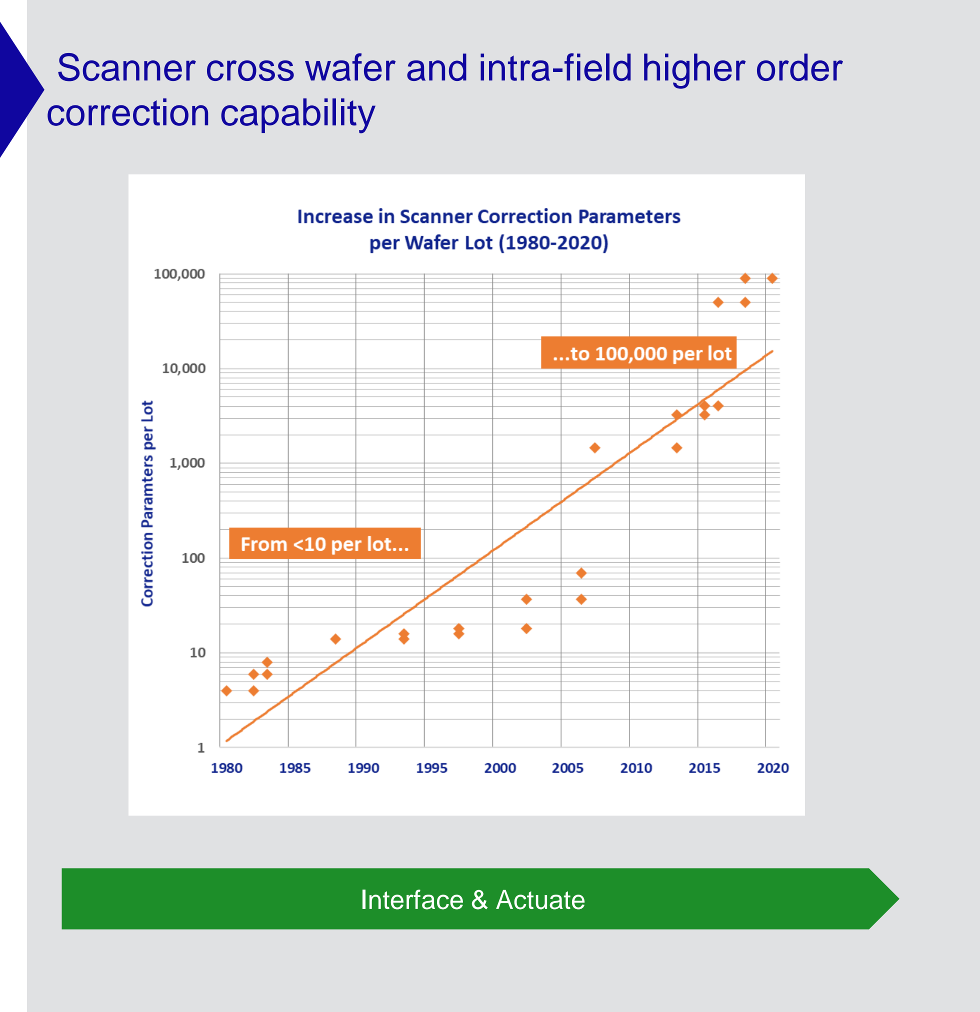
Public

Massive* metrology required for higher order EPE scanner correction

and parts per billion defect control based on local effects





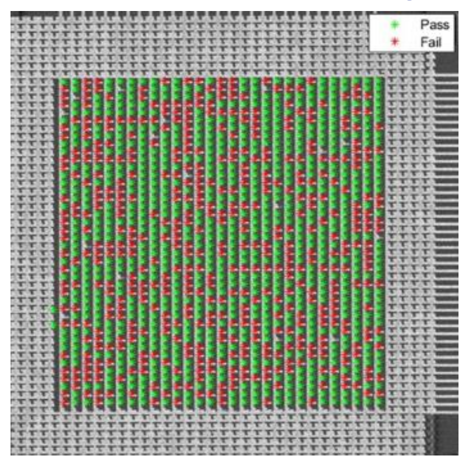


* Spatially dense; time frequency in HVM tbd

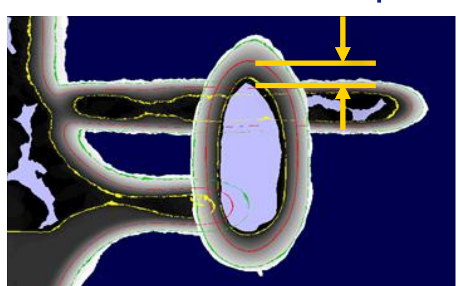
Public

EPE metric shows direct correlation to electrical failures detected by VC inspection, enabling inline EPE monitoring and control

Y-axis (VC yield): VC pass rate% per image



X-axis (EPE): measured placement error distribution median per image



EPE and VC (voltage contrast) data measured on eP5

VC Pass rate vs. EPE metric

VC pass rate [%]

EPE [nm]

VC image

Open

VC image

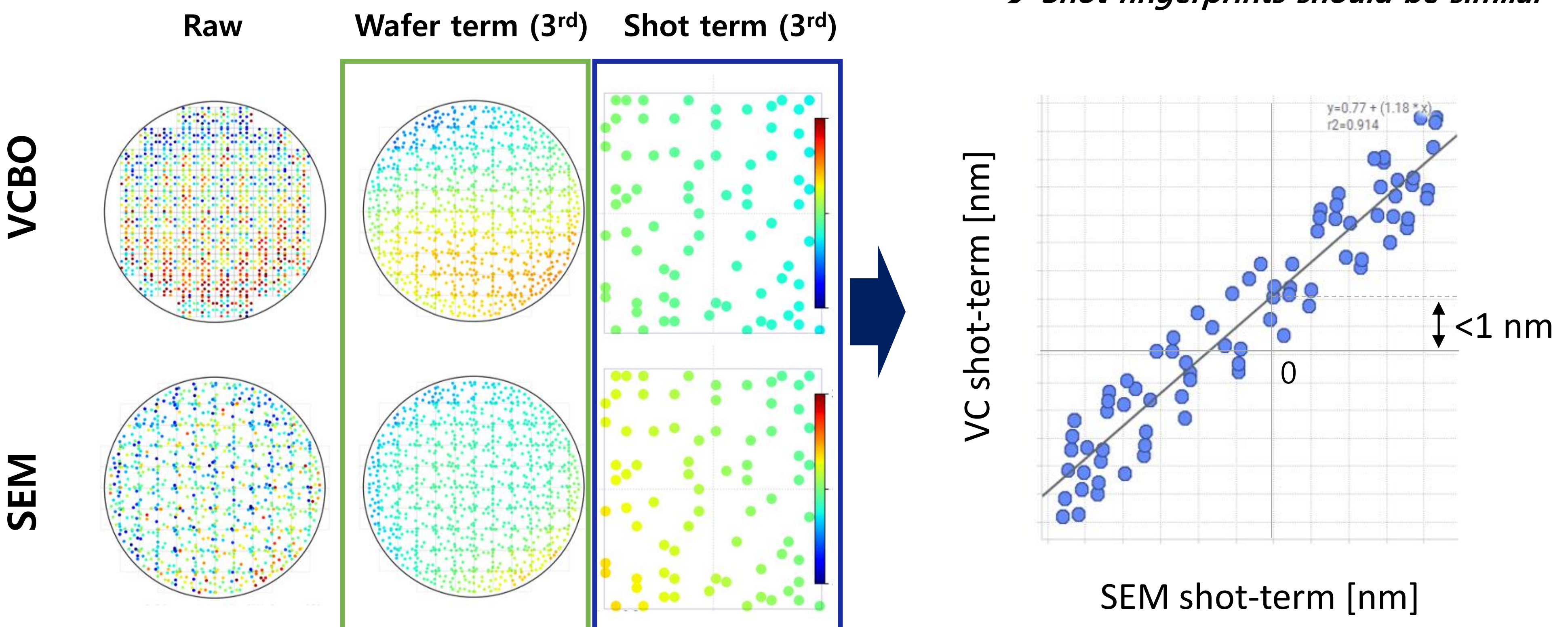
Short

SAMSUNG ASML

Comparison with SEM based in-die overlay

- There is an offset (<1nm) between VCBO and SEM
- Wafer fingerprints show difference
- Shot fingerprints are well matched

Expected results!
➔ **A discrepancy of VCBO and SEM is likely to come from non-photo process, e.g., filling, which cannot make shot-like fingerprints**
➔ ***Shot fingerprints should be similar***



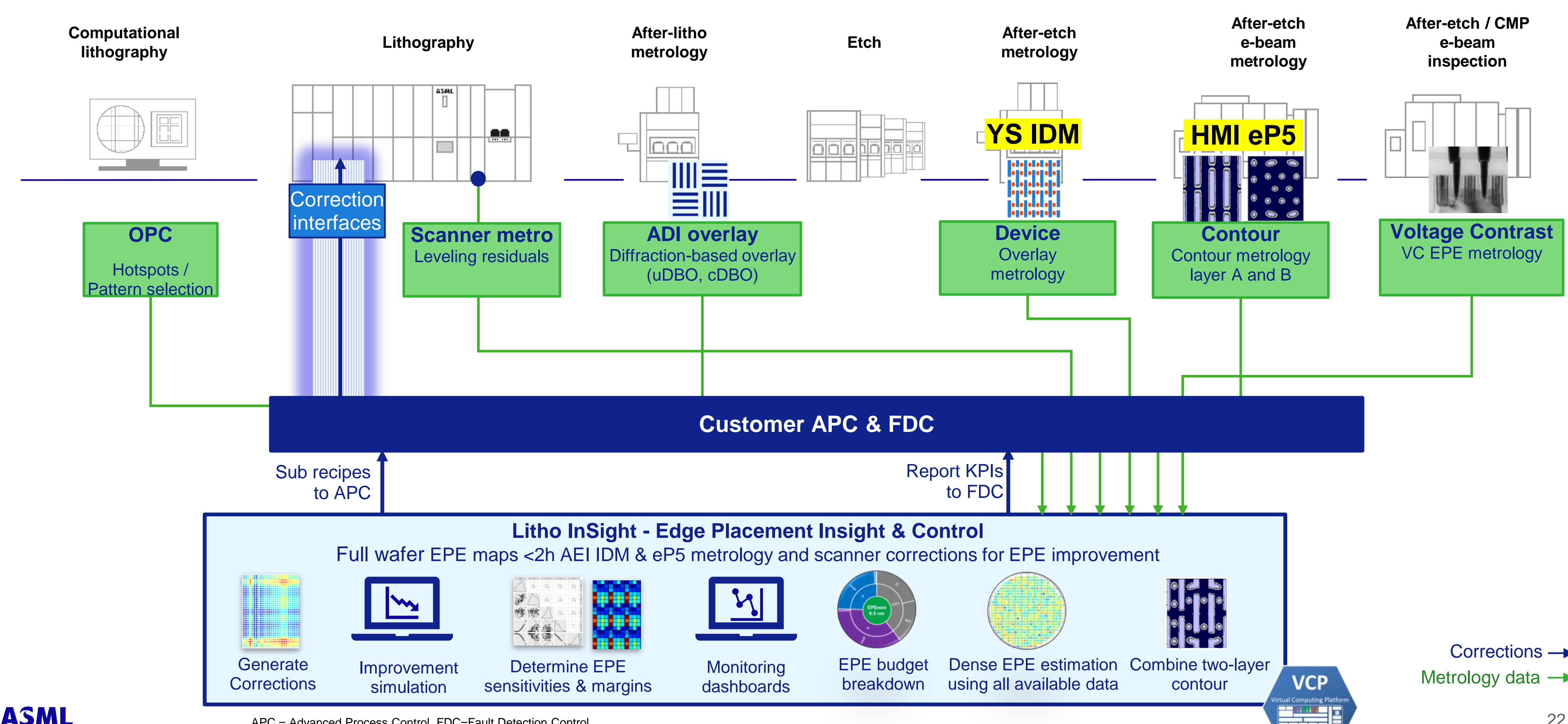
All scaled same

Moosong Lee et al. "Absolute overlay measurement based on voltage contrast defect inspection with programmed misalignments for DRAM devices," Proc. SPIE 12053, 1205315, 2022 (Best Paper)

Public

EPE monitoring & optimization enabled by solid metrology platform

combination of YieldStar device overlay metrology and HMI e-beam CD metrology data



APC = Advanced Process Control, FDC=Fault Detection Control

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ASML e-beam papers at SPIE 2023

12494-36 Reducing single layer EPE variations in EUV Lithography

Author(s): Jo Finders et al.

2 March 2023 • 8:00 AM - 8:20 AM PST | Convention Center, Grand Ballroom 220A

12495-42 Voltage contrast evaluation of dual-damascene 28nm-pitch EUV patterning and via overlap (Invited Paper)

Author(s): Etienne De Poortere et al.

2 March 2023 • 9:30 AM - 10:00 AM PST | Convention Center, Room 210A

12496-20 EPE-aware process optimization for scanner dose and overlay in DRAM use case

Author(s): Inho Kwak et al.

28 February 2023 • 1:30 PM - 1:50 PM PST | Convention Center, Grand Ballroom 220B

12496-21 The edge placement error characterization and optimization for advanced logic and DRAM nodes

Author(s): Harm Dillen et al.

28 February 2023 • 1:50 PM - 2:10 PM PST | Convention Center, Grand Ballroom 220B

12496-103 Depth estimation from SEM images using deep learning and angular data diversity

Author(s): Tim Houben et al.

1 March 2023 • 4:10 PM - 4:30 PM PST | Convention Center, Grand Ballroom 220B

12496-133 Large field of view metrology: detecting critical edge placement error signatures not seen with small field of view in an HVM environment

Author(s): Mohamed Ridane et al.

On demand | Presenting live 1 March 2023