DFEB Methodology Guidelines for Physical Design Engineers

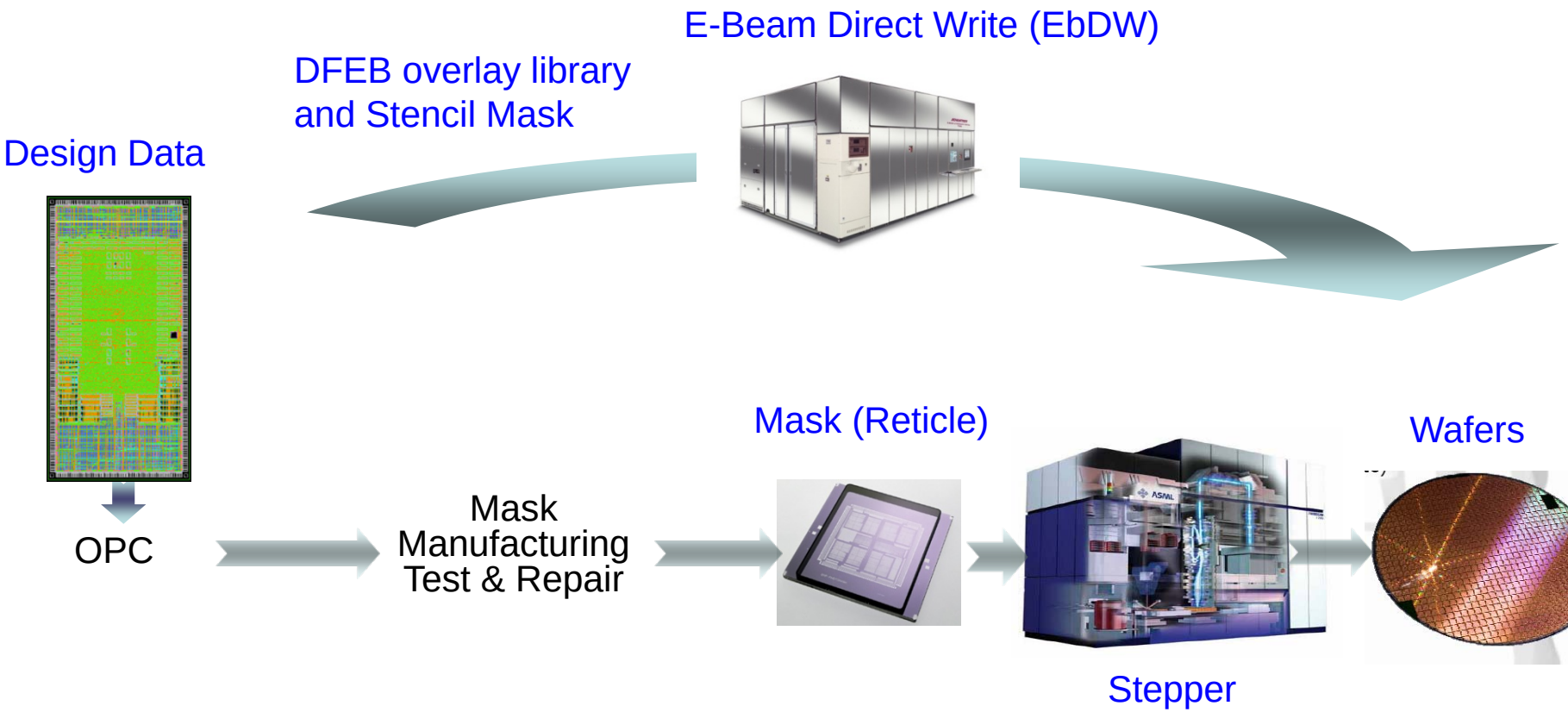
Revision 2.1 November 9, 2009

Content

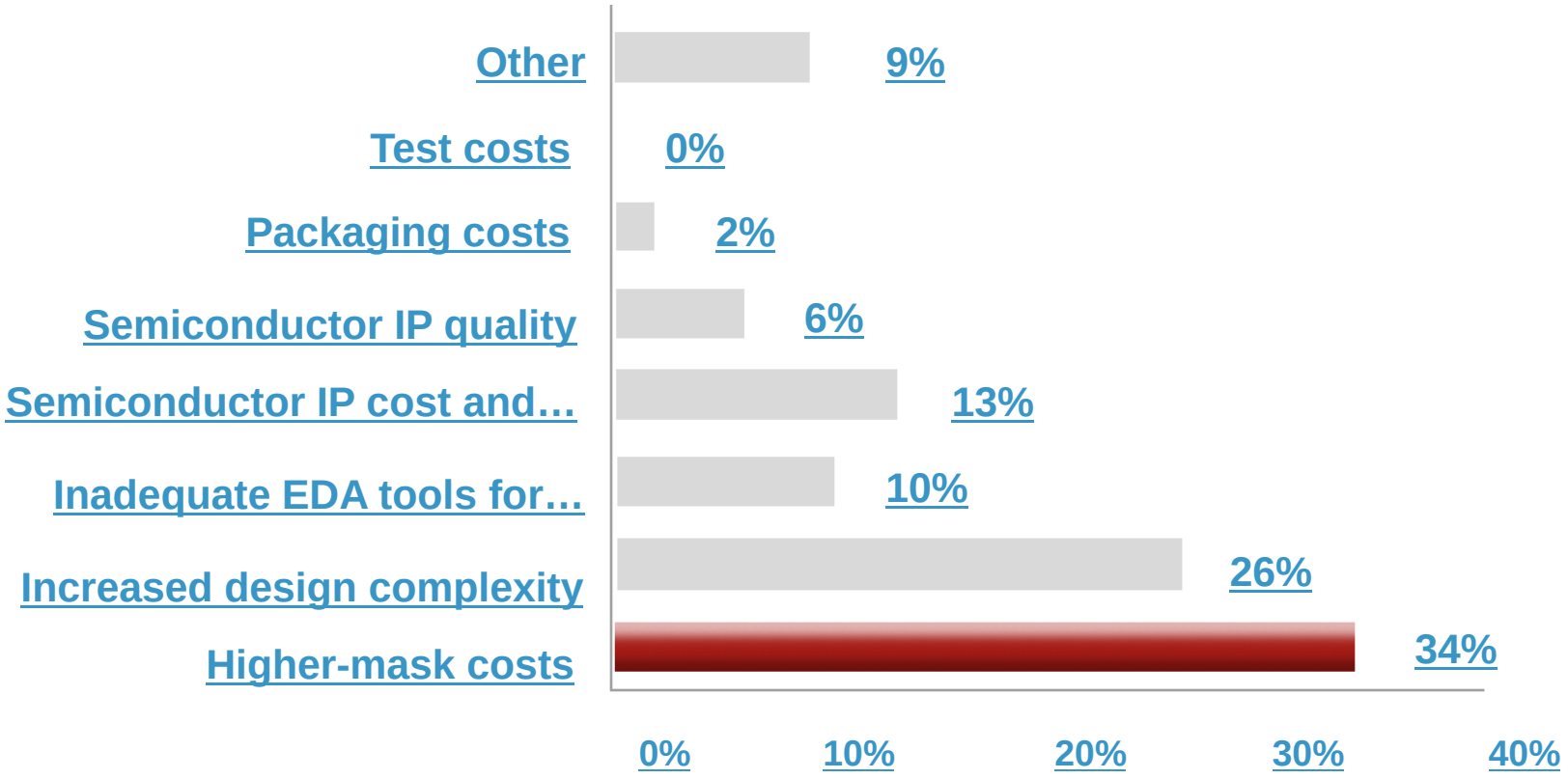
- Design for E-Beam: What and Why
- Shot Count Analysis
- Synthesis Best Practices for DFEB
- Place & Route Best Practices for DFEB

Design for E-Beam (DFEB): What and Why

DFEB vs. Mask Manufacturing Process

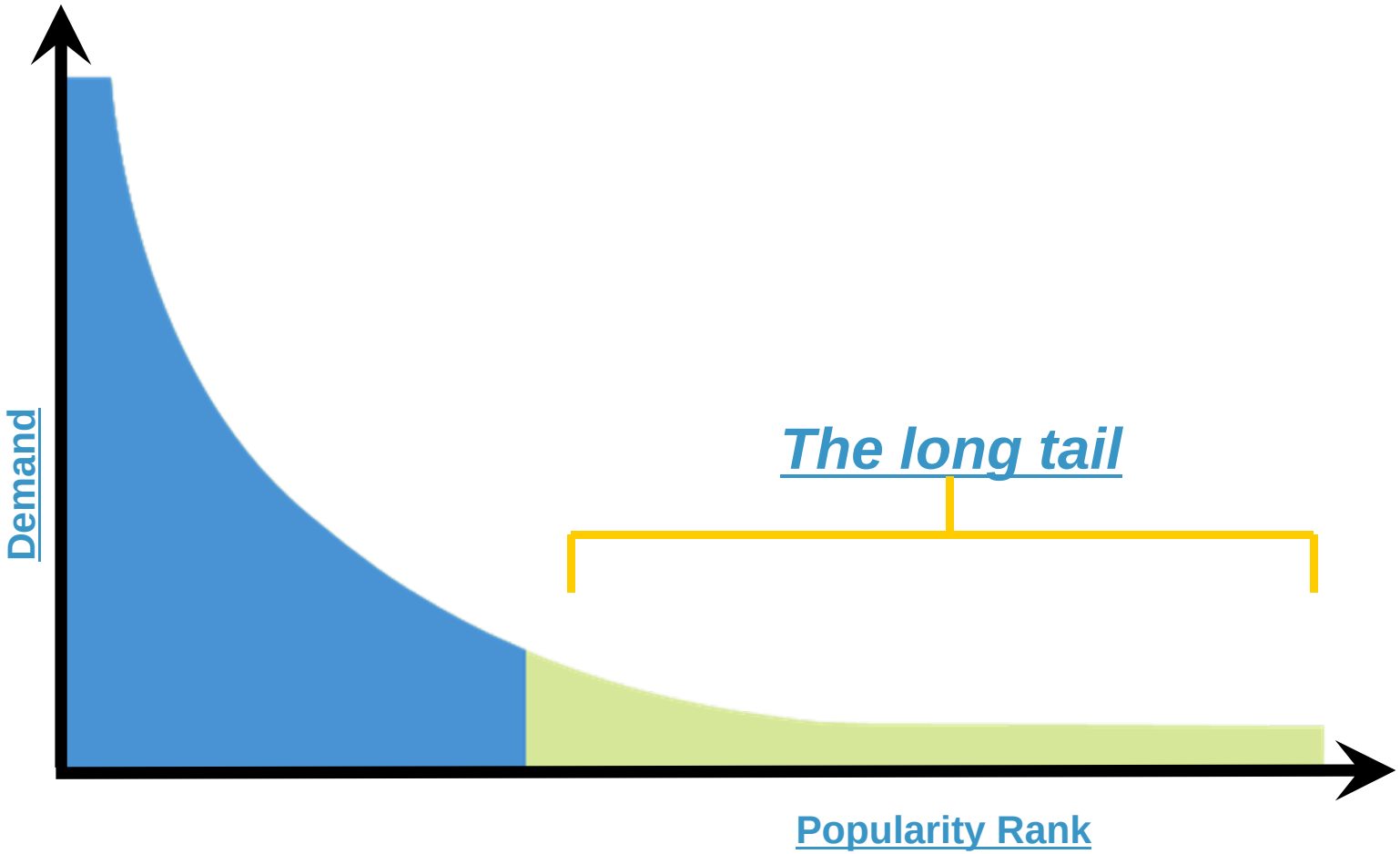


Mask Cost is Top Concern



Source: Global Semiconductor Association (GSA) member survey, December 2007

Enabling the Long Tail of SoCs



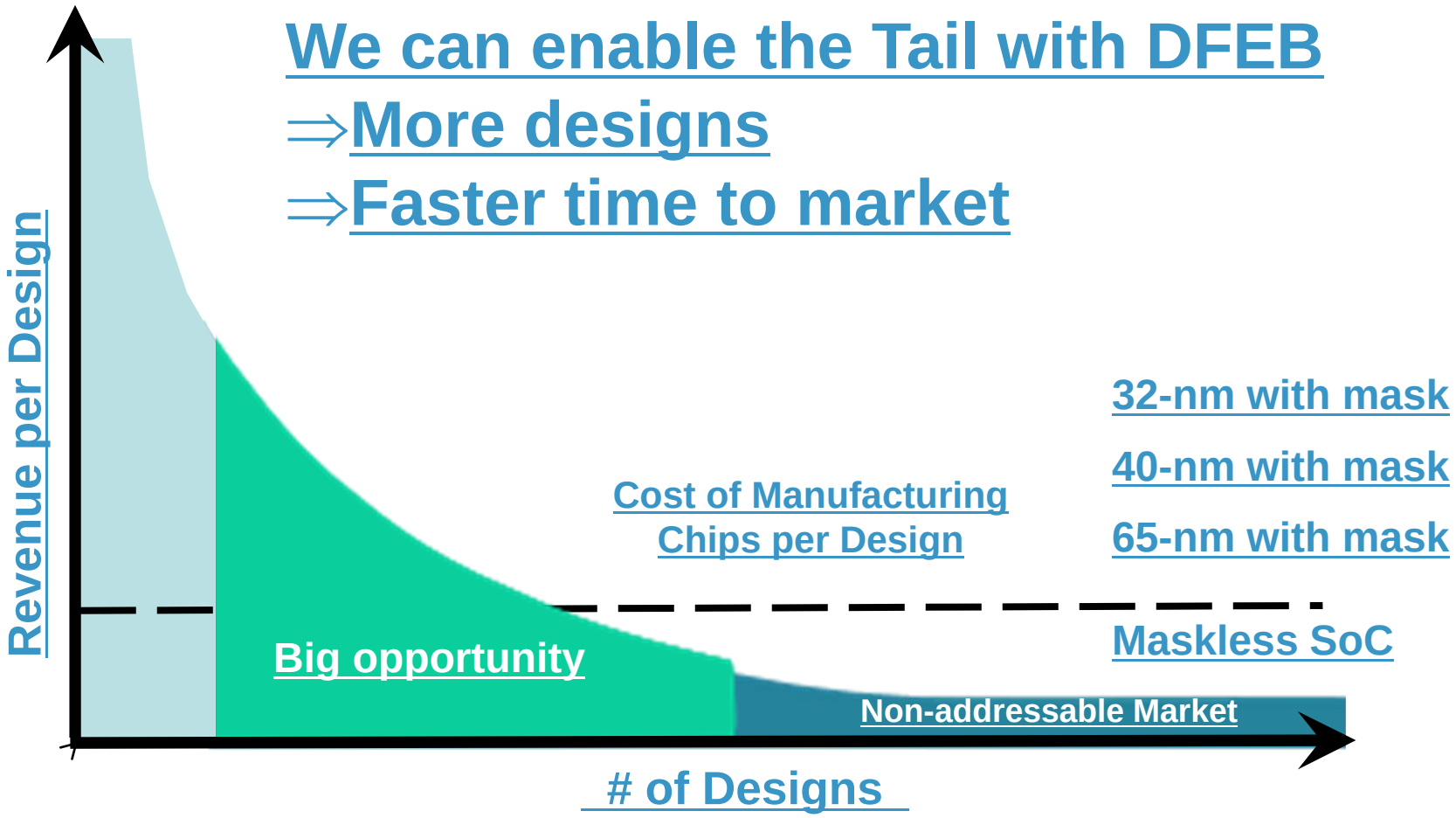
Source: Chris Anderson's "The long tail: Why the future of business is selling less of more"

The Tail is Getting Shorter

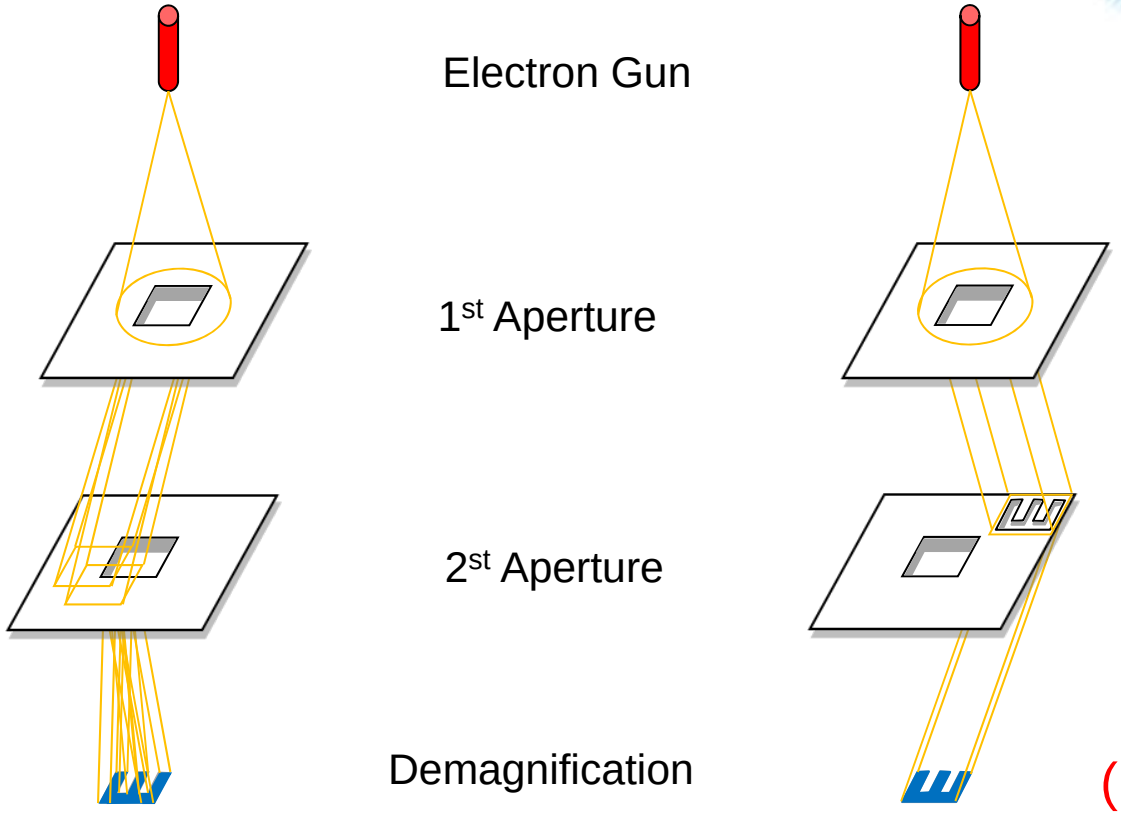
We can enable the Tail with DFEB

⇒More designs

⇒Faster time to market



DFEB Uses Character Projection



(4 shots)

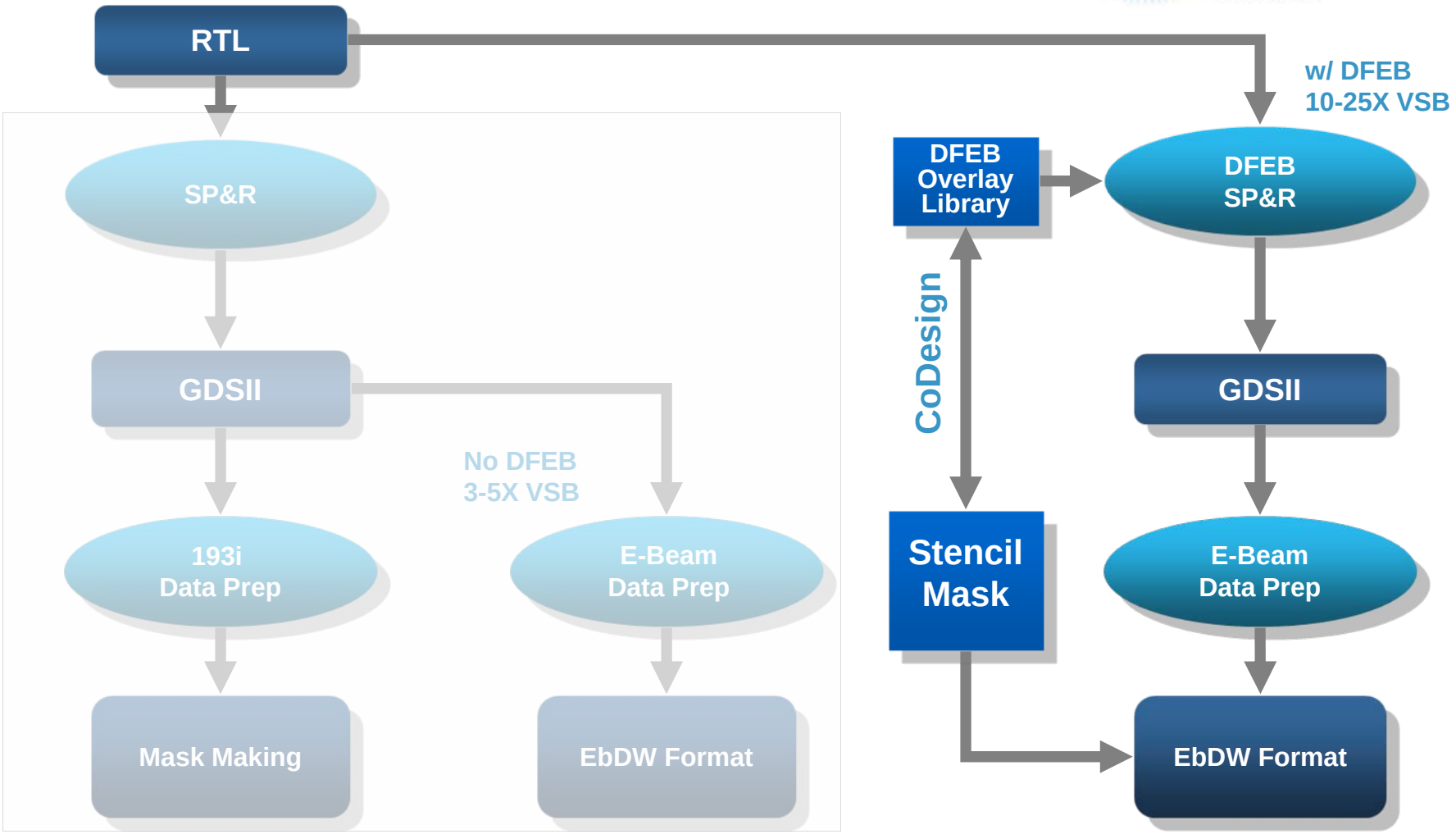
Variable Shape Beam (VSB)

(1 shot)

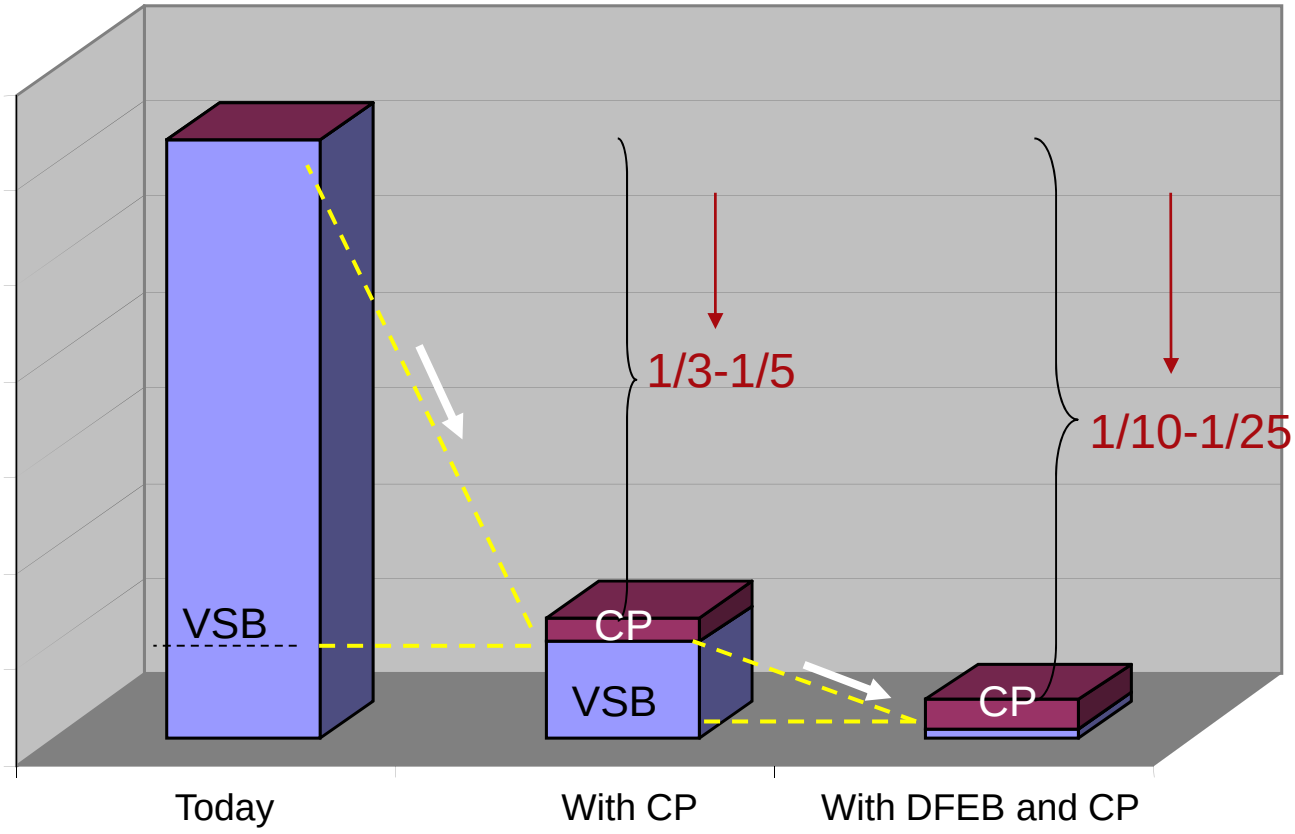
Character Projection (CP)

Drawing Courtesy Hitachi High-Technologies

DFEB Overview



DFEB Increases Throughput
by Decreasing Shots

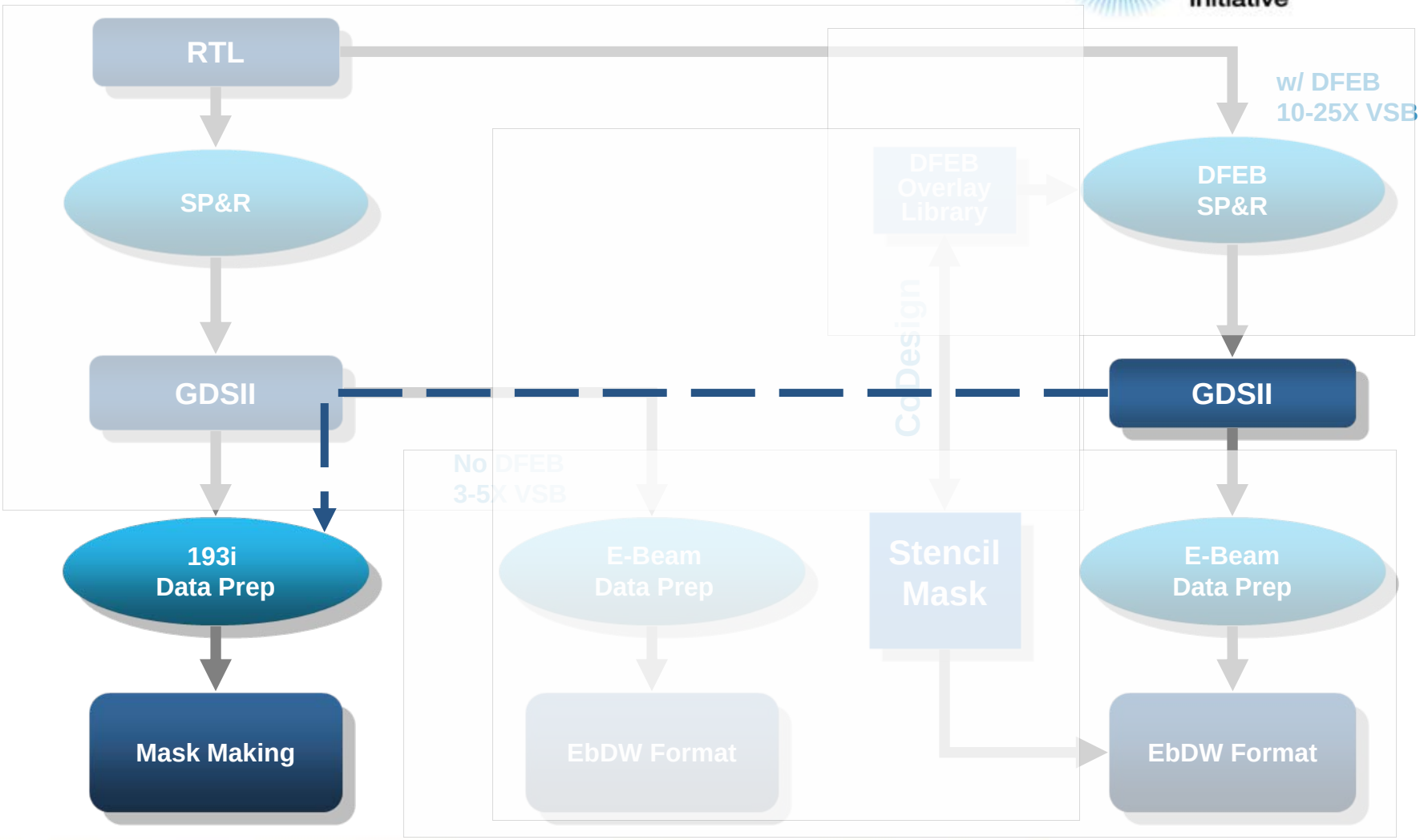


DFEB achieves a 10-25X reduction by:

1. Co-designing the cell library and the stencil mask
2. Optimizing the physical design for CP

Comparison Source: D2S, Inc. Computer simulation of e-beam write time on a particular test case (speed up is dependent on aperture size and utilization %)

DFEB Designs Are Compatible With Mask-based Volume Productions



Shot Count Analysis

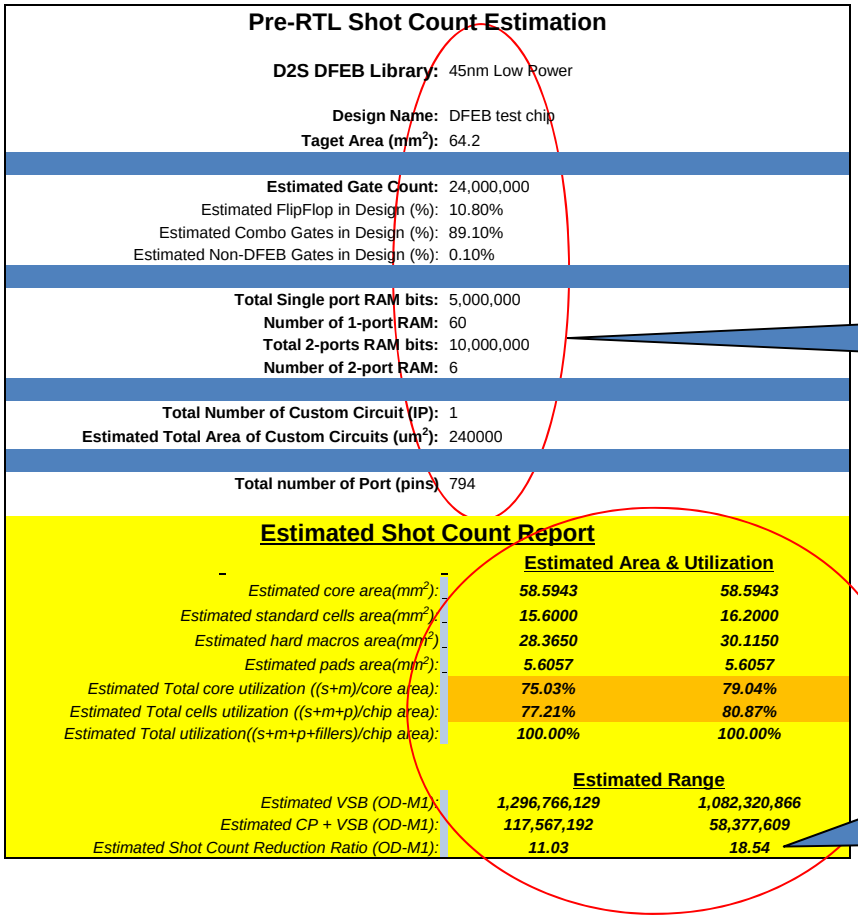
Terminology Clarification

- “Generic” flow/steps: Refers to the flow you are already using
- “DFEB” flow/steps: Additional steps or data needed to augment the generic flow for DFEB

Why Shot Count Is So Important

- Generic flow optimizes for area, timing, yield and power
- In DFEB flow, also optimize for shot count
  - Goal is defined at the beginning of the design
- Run shot count analysis at multiple points in the flow
  - Design flow checkpoint
  - Monitor and evaluate the cost of design trade-offs
- Shot count reports are refined in each step throughout the flow

Pre-RTL Shot Count Analysis Worksheet



Pre-RTL Shot Count Estimation

D2S DFEB Library:	45nm Low Power
Design Name:	DFEB test chip
Taget Area (mm^2):	64.2
Estimated Gate Count:	24,000,000
Estimated FlipFlop in Design (%):	10.80%
Estimated Combo Gates in Design (%):	89.10%
Estimated Non-DFEB Gates in Design (%):	0.10%
Total Single port RAM bits:	5,000,000
Number of 1-port RAM:	60
Total 2-ports RAM bits:	10,000,000
Number of 2-port RAM:	6
Total Number of Custom Circuit (IP):	1
Estimated Total Area of Custom Circuits (um^2):	240000
Total number of Port (pins)	794

Estimated Shot Count Report

	Estimated Area & Utilization	
Estimated core area(mm^2):	***58.5943***	***58.5943***
Estimated standard cells area(mm^2):	***15.6000***	***16.2000***
Estimated hard macros area(mm^2):	***28.3650***	***30.1150***
Estimated pads area(mm^2):	***5.6057***	***5.6057***
Estimated Total core utilization ((s+m)/core area):	***75.03%***	***79.04%***
Estimated Total cells utilization ((s+m+p)/chip area):	***77.21%***	***80.87%***
Estimated Total utilization((s+m+p+fillers)/chip area):	***100.00%***	***100.00%***
	Estimated Range	
Estimated VSB (OD-M1):	***1,296,766,129***	***1,082,320,866***
Estimated CP + VSB (OD-M1):	***117,567,192***	***58,377,609***
Estimated Shot Count Reduction Ratio (OD-M1):	***11.03***	***18.54***

Excel spreadsheet already prepared and available for use for shot count analysis

Parameter entries are based on Design Specification

Shot Count Analysis report output includes shot count for VSB, CP+VSB, and provides the range of shot count reduction ratios. **Use this as the shot count goal.**

Shot Count Report Example

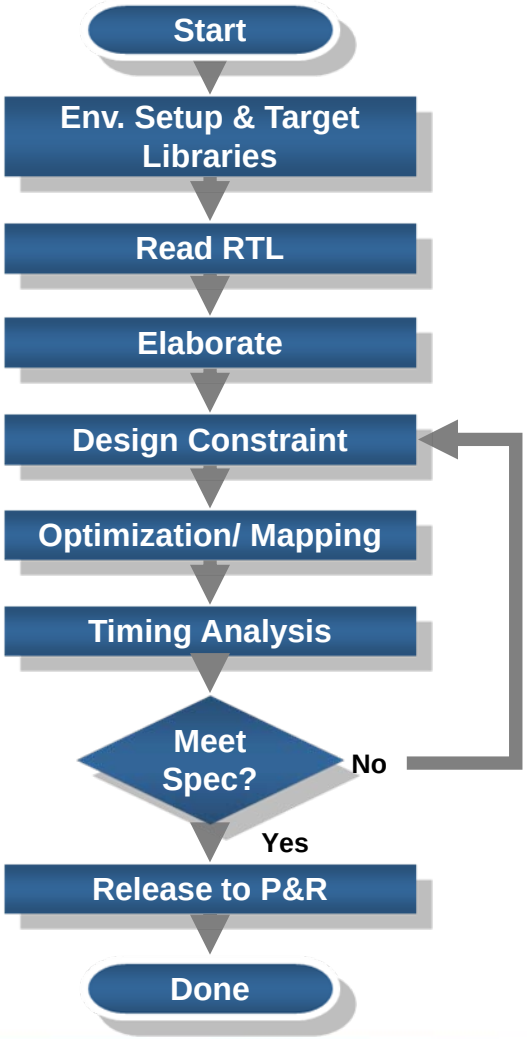
Model	Count	CP Shot	Total VSB Shots	Total DFEB Shots
OAI22X6_D2S	6533	4	326650	26132
IVX1_D2S	20137	4	583973	80548
….				
SDFFRP_D2S	17461	8	5011307	139688
….				
Total	320793		27138554	1681143

Reduction Reports

Shot Count Reduction Ratio (Cells): 16.14

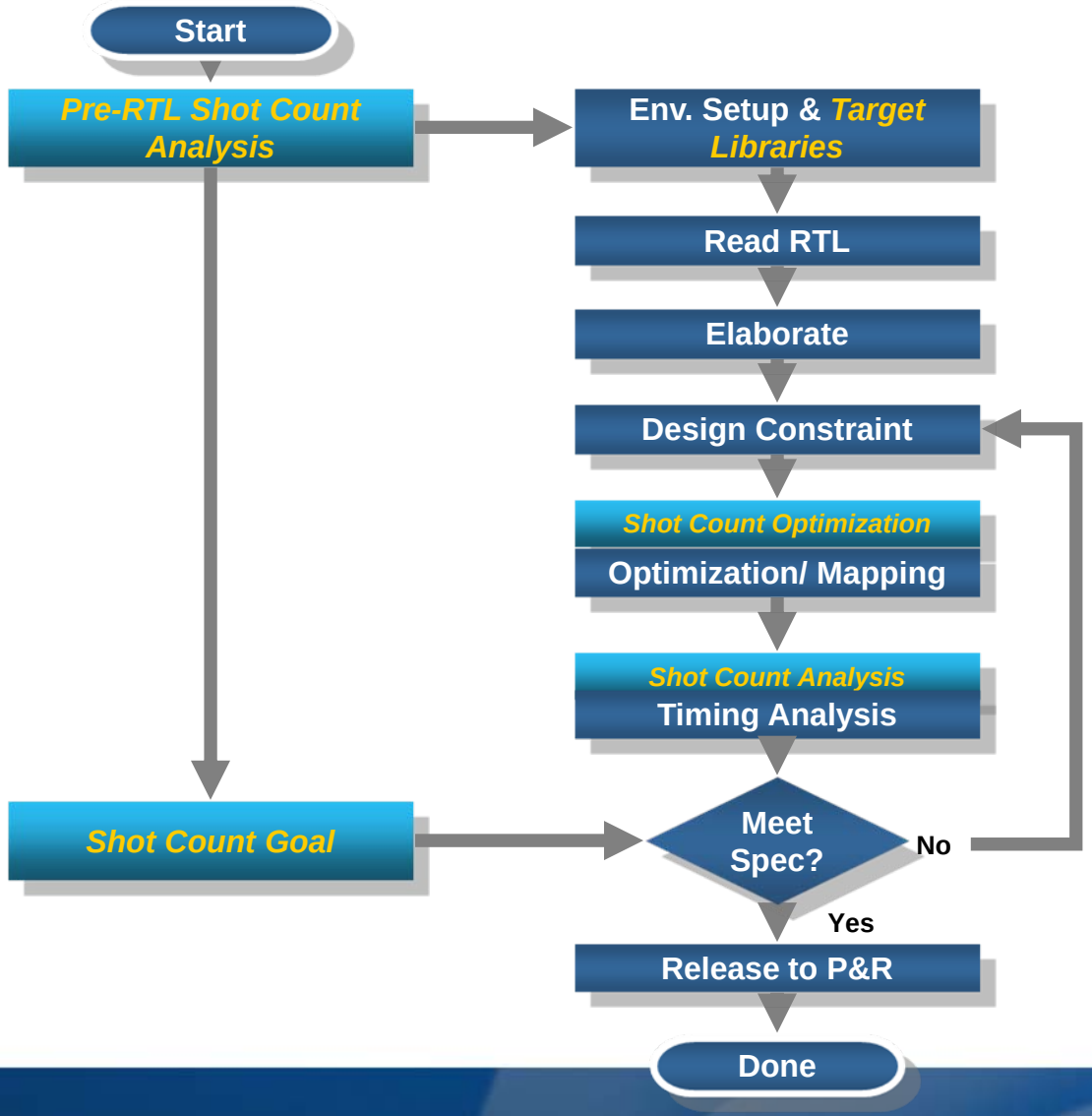
Synthesis Best Practices for DFEB

Generic Synthesis Flow



Generic RTL synthesis steps

DFEB Synthesis Flow



DFEB includes additional steps for shot count optimization and analysis

What Is NOT Changed

- No change to RTL
- No change to SDC constraint files
  - Same ECO refinement process used to get design to meet the Area, Timing, and Power.
- No change to timing analysis scripts or commands

DFEB Synthesis Steps

Environment & Library Setup

- Add DFEB overlay library to the target generic libraries

Otherwise the same as the generic synthesis tools setup

Import RTL Netlist and Elaborate

- Perform generic procedure to read in the RTL
- Elaborate the design
- Perform generic procedure to read in SDC constraints

Shot Count Optimization

- Prior to optimization and mapping, run shot count optimization setup script to set additional constraints to prefer DFEB overlay library cells
- Run generic optimization/mapping command to perform timing, area, and power optimization

Shot Count Analysis

- After optimization, run shot count analysis to:
  - Reset the cell attributes so that other reports are accurate
  - Generate a shot count report
- Compare the shot count reported to the shot count goal
  - Shot count analysis is based on cell count without taking wire routing, filler cells, and well taps in consideration
- Then run timing analysis and other reports

Synthesis ECO

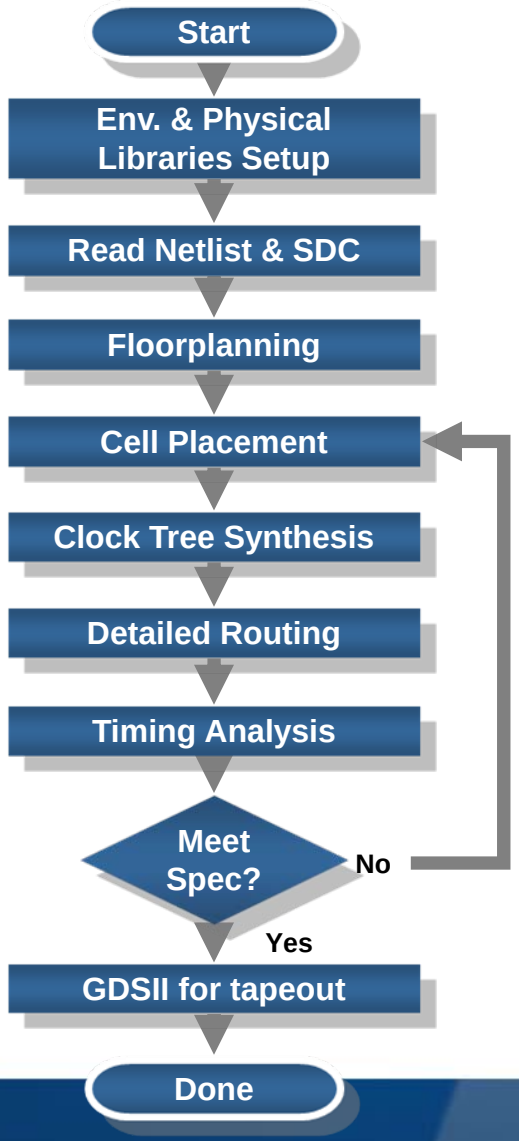
- Perform ECO to fix critical timing, area, or power issues with these in mind:
  - Based on DFEB constraints, virtually all cells will be DFEB overlay library cells
  - Where necessary, fix critical timing paths using non-DFEB (generic) cells with better performance at the cost of increased shot count

Release to Place & Route

- Release to place & route when timing, area, power and shot count goals are met
- Generate SDC for P&R tools as you would in generic flow

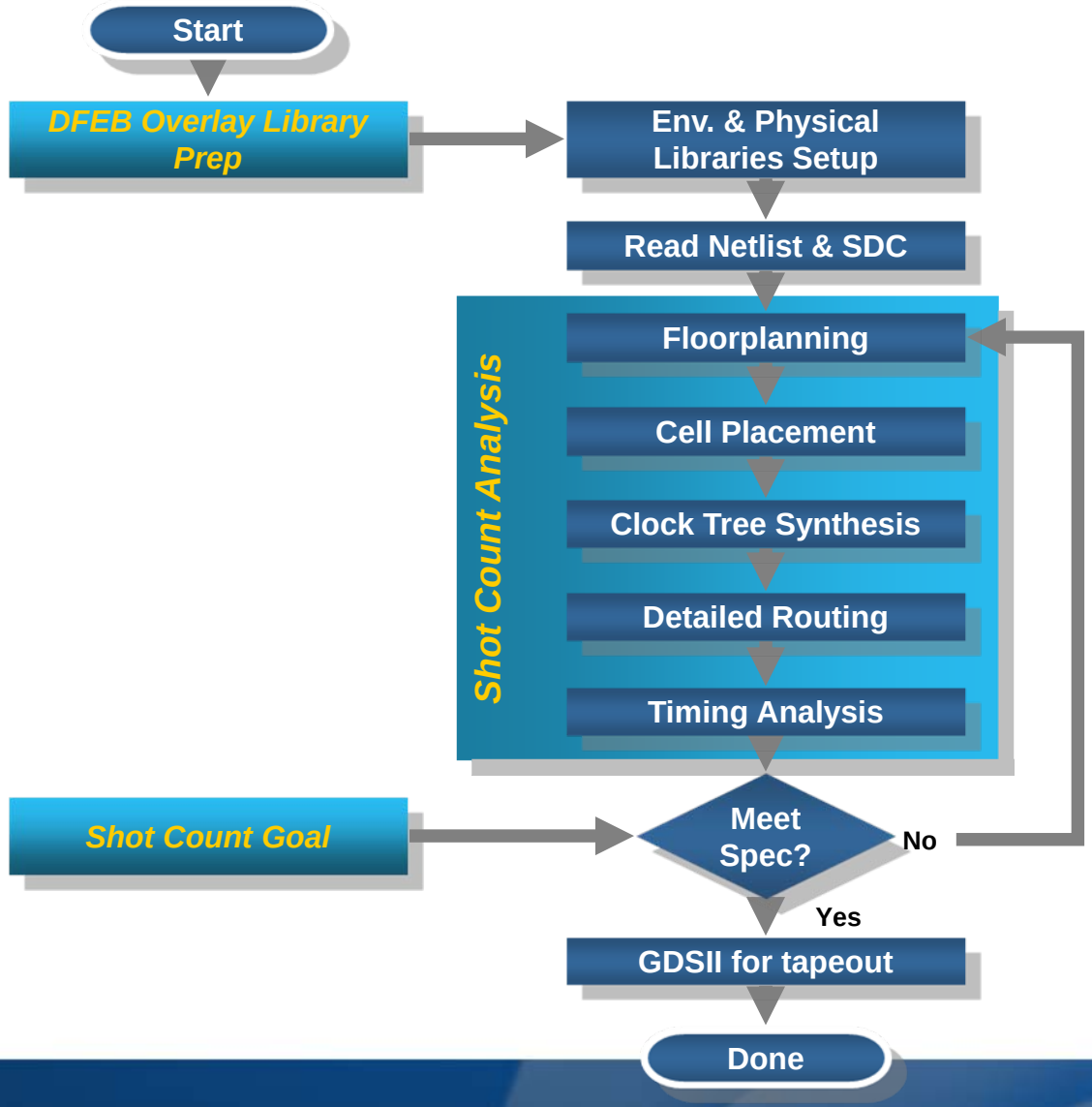
Place & Route
Best Practices for DFEB

Generic Place & Route Flow



Generic Place & Route steps

DFEB Place & Route Flow



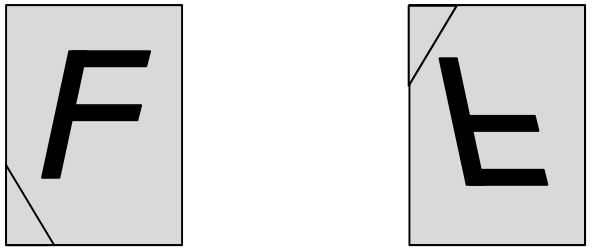
DFEB includes additional steps for shot count optimization and analysis

DFEB Overlay Library Preparation

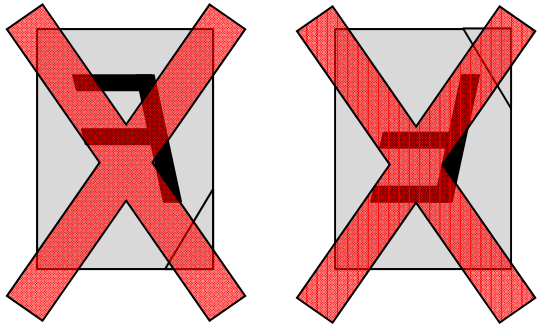
- Purpose: minimize shot count
- Set the following attributes in the DFEB overlay library to make them the default for the tools:
  - Orientation preference
  - Pin access and connection preference
  - Metal1 routing preference
- Can always override attributes if needed (to meet other constraints)

Orientation Preference

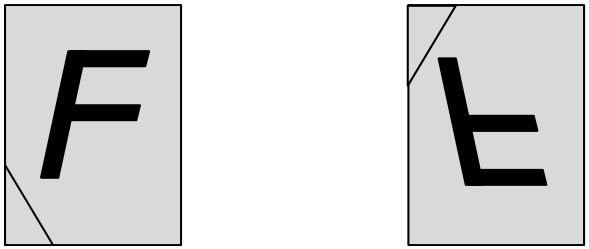
- North or Flip-South orientation is preferred for standard cells



North (R0) Flip-South (MX)



- North or Flip-South orientation is preferred for RAM/ROM macros

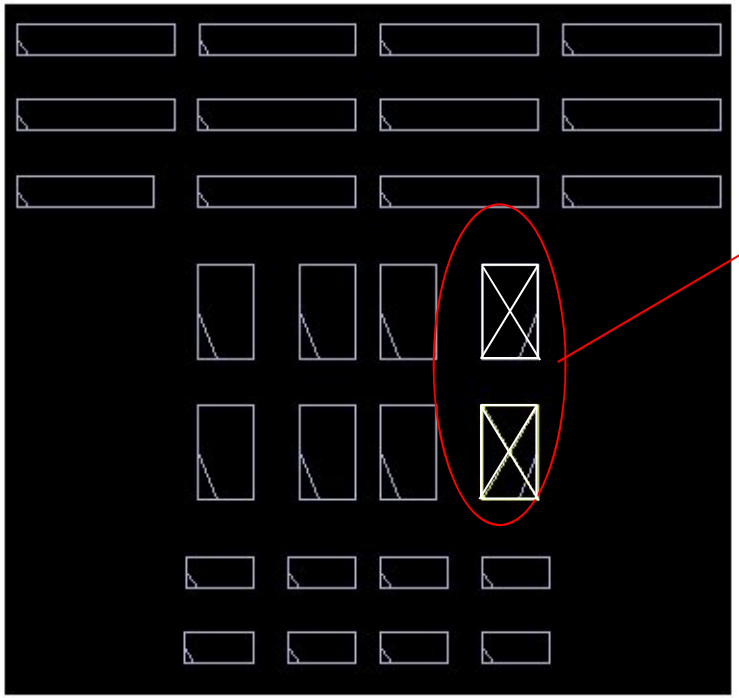


North (R0) Flip-South (MX)

Shot count Warning:

Standard cells and RAM/ROM macros that do not follow the predefined orientations will be shot with VSB instead of CP, increasing shot count.

Floorplanning Examples

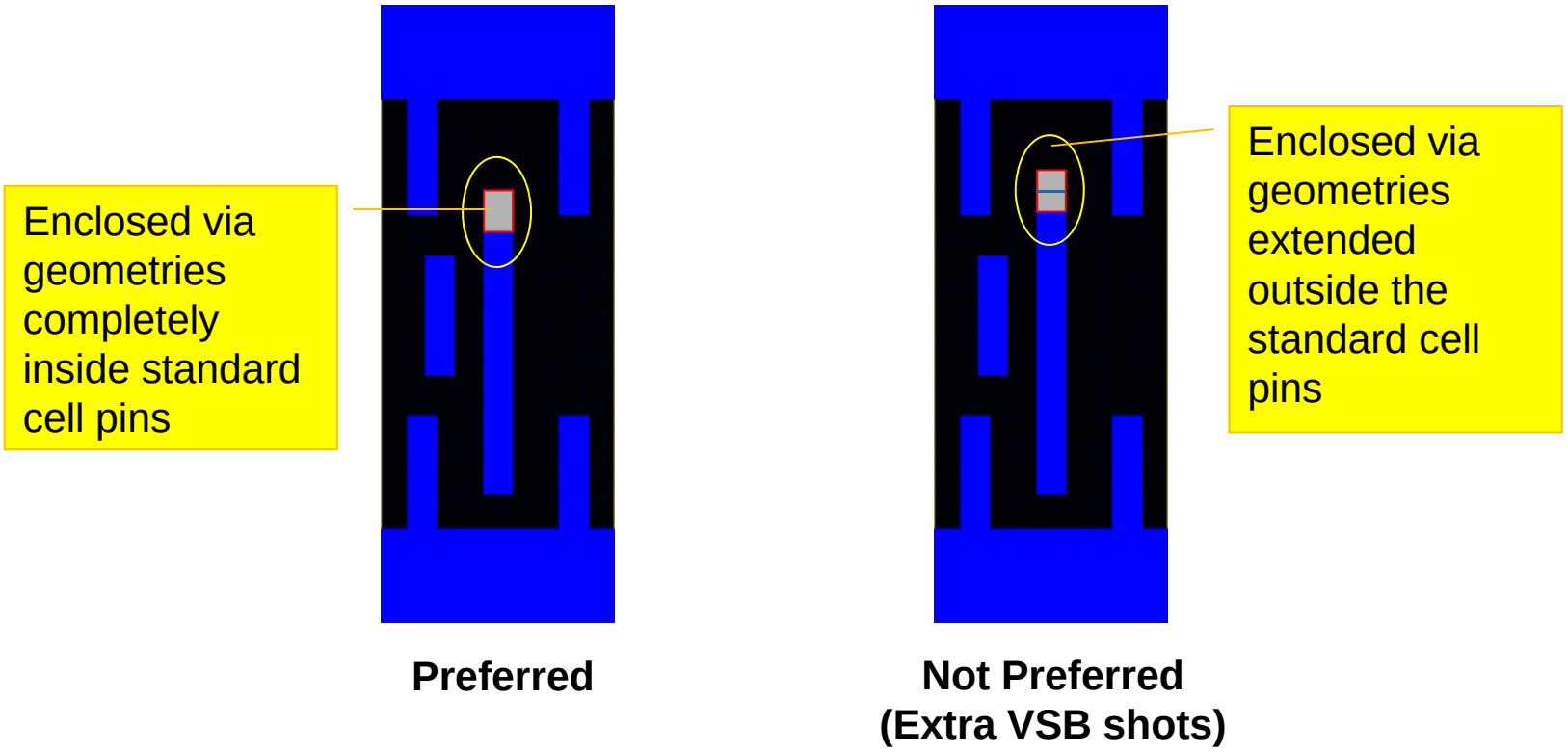


- RAMs with non-preferred orientation will be shot with VSB, and therefore increase the shot count.
- Trade off is between congestion and shot count.

Recommended:

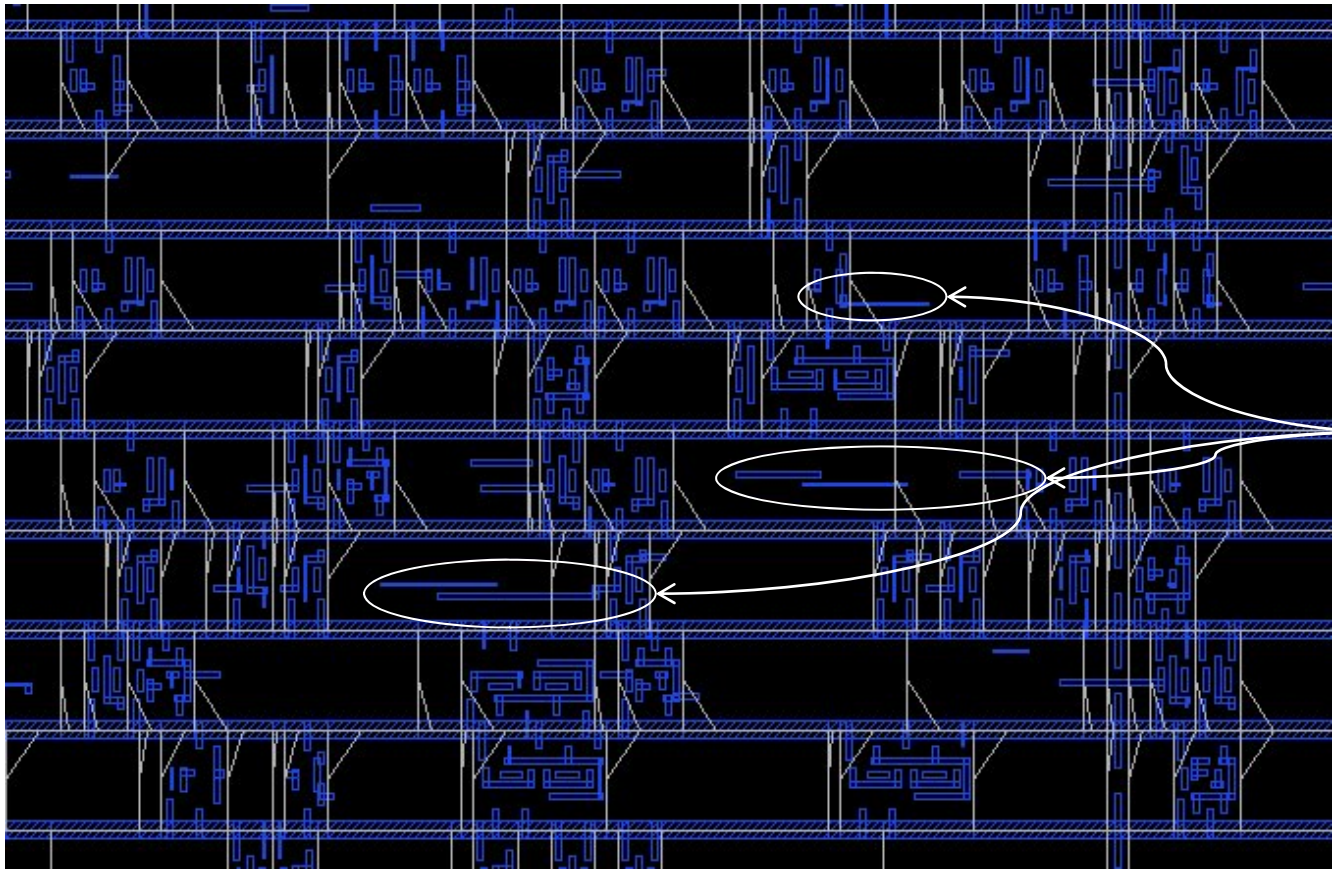
Use non-preferred orientation only when needed to relieve routing congestion.

Pin Access and Via Drop Preferences



- Refer to the P&R tools documentation for routing options to drop vias inside the standard cell pins

Metal1 Routing Preferences

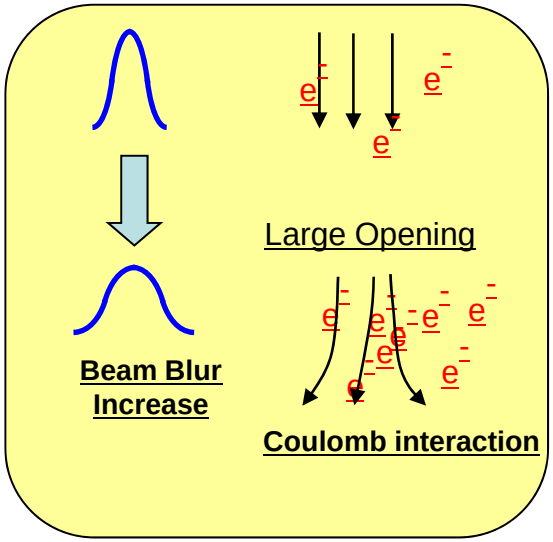


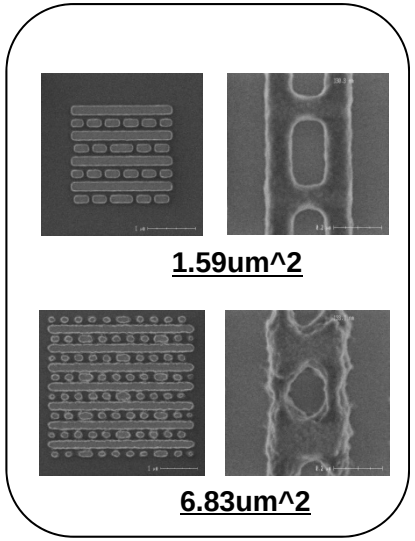
- Metal1 stub routes will increase shot count

Shot count Warning:

Avoid Metal1 Stub Routing (Use tools option to turn off these types of routing)

A Bit of Background



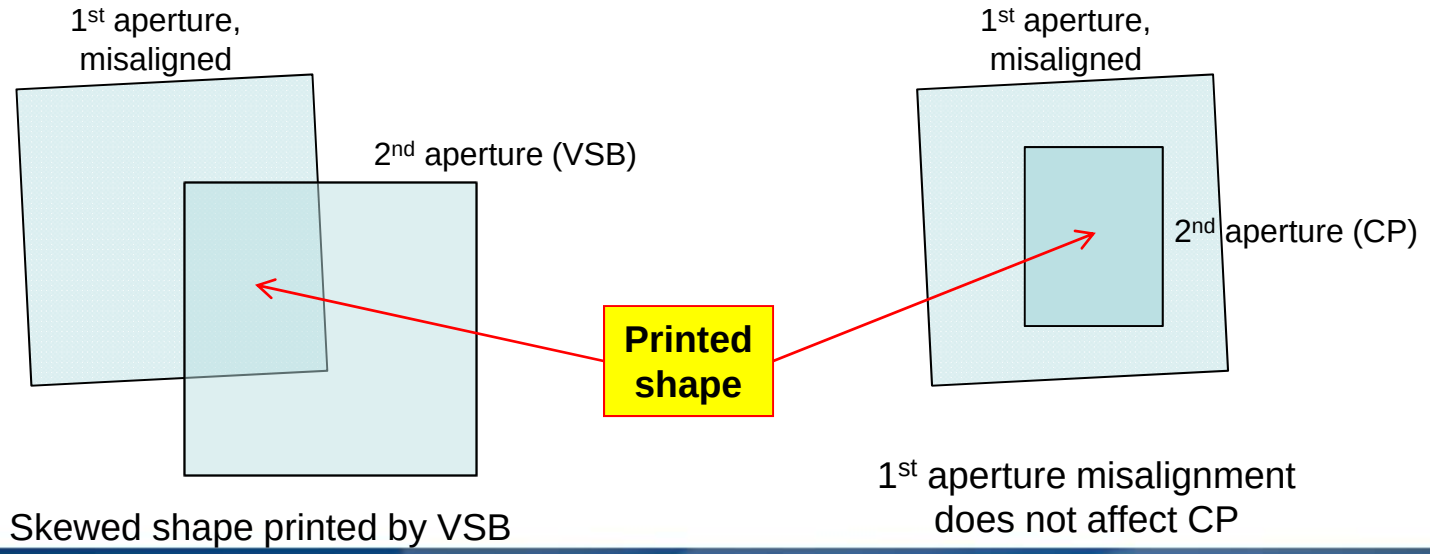


- Electrons in an e-beam repel each other
- As an e-beam becomes larger, printed image gets more blurred (see picture on right)
- Using close to maximum allowed e-beam size is important for less shot count.

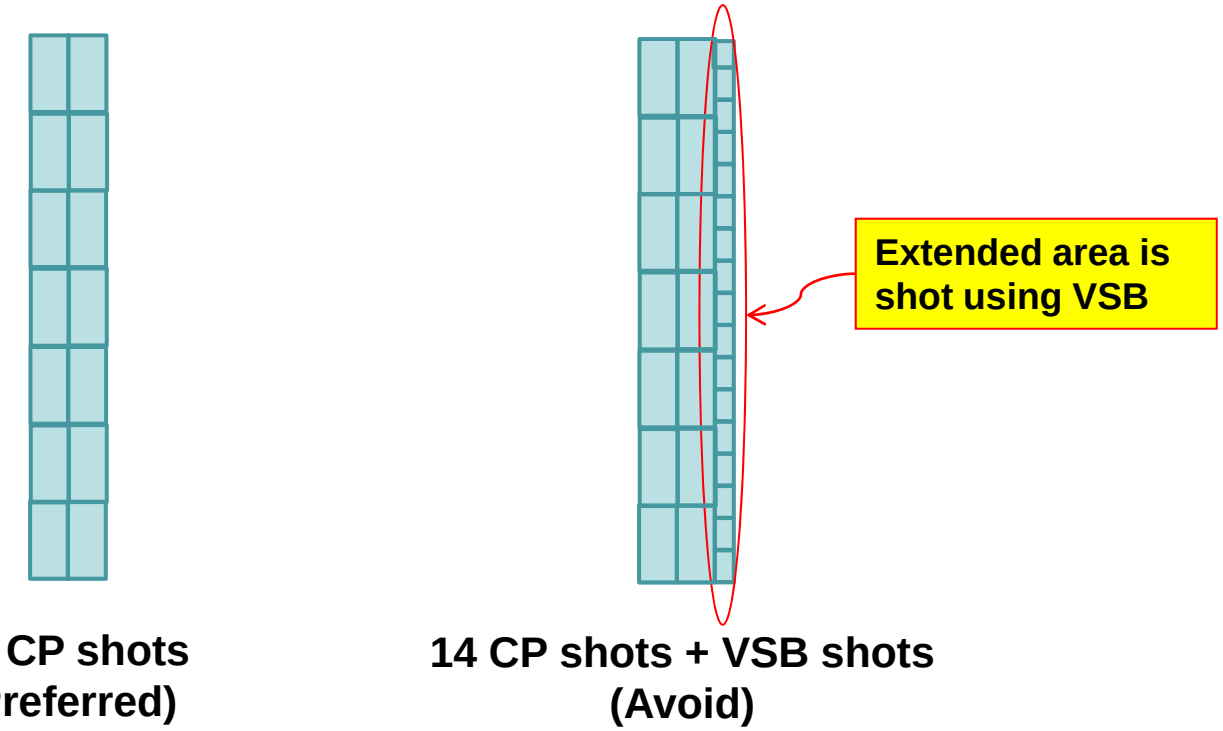
Source: Maruyama, et.al., EIPBN 2009

Power Routing Has High Impact on Shot Count

- Power routing is a very large area
- The Coulomb effect dictates the maximum area per shot
- CP can write wires longer than 2µm more accurately than VSB
  - Due to possible misalignment of first and second apertures for VSB
  - CP relies on the shape of the stencil alone

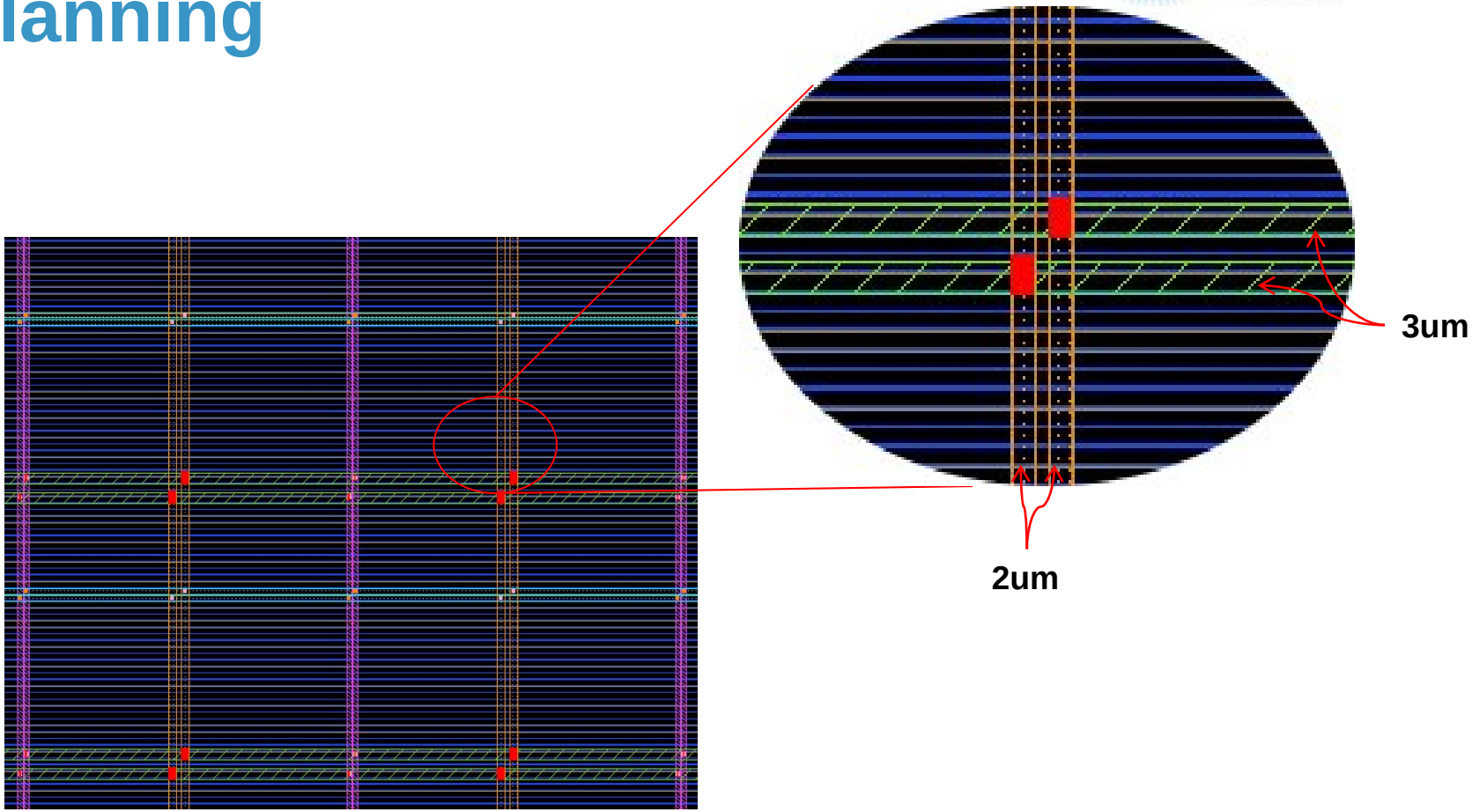


Power Grid Planning Using Wide Metals



- Choose a unit width, and use whole multiples of this width
- Fewer, wider power stripes result in lower shot count

Example of Power Grid Planning



- Wide metals have widths of 2µm and 3µm (whole multiples of 1µm)

Cell Placement

- Perform generic cell placement step
- Shot count analysis after this step produces shot count report excluding shot count used for routing layers.

Clock Tree Synthesis (CTS)

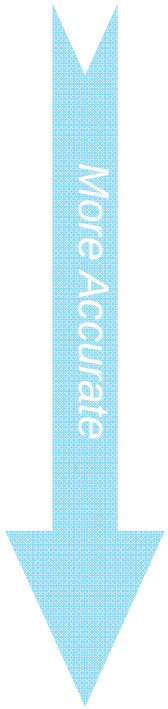
- Specify buffers, inverters, and delay cells from the DFEB overlay library
- Perform CTS using the above DFEB cells
- Shot count analysis will now include the clock tree cells

Detail Routing and Timing Closure

- Perform generic detailed routing step for timing closure
  - No M1 for routing
  - Via1 placed within a pin
  - For compatibility to photo-mask manufacturing, plan to do DFM design also
- Shot count analysis will now include the detail routing

Shot Count Analysis Accuracy

Shot count reports are refined in each step



Pre-RTL shot count analysis	Excel spreadsheet-based analysis. Parameter entries are based on design specification.
After synthesis	Shot count based on synthesis netlist
After power routing	Shot count includes power routing
After placement	Shot count includes cell sizing, buffer insertion, and well taps
After clock tree synthesis	Shot count includes clock tree buffers and inverters
After detail routing	Most accurate shot count report. Includes routing and filler cells.

DRC and LVS

- Perform generic DRC and LVS steps
- Export final GDSII for tape-out

Summary

- DFEB flow and DFEB overlay library enable EbDW IC manufacturing
- DFEB design methodology includes few additional steps for shot count optimization and analysis
- Shot count analysis throughout the flow monitors shot count and design trade offs
- DFEB design methodology is largely the same as a generic cell-based design methodology
- DFEB designs are fully compatible and can be manufactured with optical lithography for volume production

Summary of Abbreviations

CP	Character Projection
DFEB	Design for E-Beam
EbDW	E-beam Direct Write
VSB	Variable Shape Beam


eBeam
Initiative