IMAGINE: an open consortium to boost maskless lithography take off First assessment results on MAPPER technology

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ABSTRACT

In the latest ITRS roadmap updated in July 2010, Maskless remains identified as one of the candidate to address lithography needs for the sub-16nm technology nodes. The attractiveness of this solution in terms of cost and flexibility linked to the throughput potential of the massively parallel writing solutions maintain the interest of large scale IC manufacturers, such as TSMC[(1)] and STMicroelectronics, to push the development of this technology. In July 2009, LETI and MAPPER have initiated an open collaborative program IMAGINE focused on the assessment of the MAPPER technology. This paper reports on the key results obtained during this first assessment year in terms of: resolution capabilities, stitching performances, technology reliability and infrastructure development. It also provides an extensive overview on the maturity degree and the ability of this low energy accelerating voltage multibeam option to answer to the industry needs in the 2015 horizon.

KEYWORDS : lithography, multi beam, low energy, photoresist, mask less

1. INTRODUCTION

In the latest ITRS roadmap updated last July 2010, Maskless remains as one of the candidate to address lithography needs for the sub-16nm technology nodes. The attractiveness of this solution in terms of cost and flexibility linked to the throughput potential of the massively parallel writing solutions maintain the interest of large scale IC manufacturers, such as TSMC[(1)] and STMicroelectronics, to push the development of this technology. Nevertheless, the development of multibeam does not reach yet the level of EUV maturity which is the other candidate for 16nm technology node. Indeed, technological solutions developed in the US, with the KLA REBL project and in Europe with IMS Nanofabrication (Austria) and MAPPER (Netherlands) are still at the pre-alpha platforms level with limited capabilities to what will be needed for the high volume manufacturing platform. But even with limited funds and supports, these companies highlighted already the potential of this technology which is now considered as a real lithography option [(2,3)].

In parallel to tool development, multibeam needs to rely on a robust infrastructure and for this partnership is essential to keep dynamic and know-how dissemination. Through its seventh framework program (FP7), from 2008 to the end of 2010, Europe has funded the first international multibeam consortium, named MAGIC, where MAPPER and IMS Nanofabrication solutions and multibeam infrastructure were jointly developed.

Starting July 2009, LETI and MAPPER have initiated an open collaborative program IMAGINE focused on the assessment of the MAPPER technology. TSMC and STMicroelectronics already joined this consortium followed by several infrastructure partners on data preparation, resist and processes. This paper briefly outlines first the objectives of this program. Then it reports the key results obtained during the first year of the MAPPER technology assessment with some focuses on tool reliability, resolution capabilities, process integration and E-Beam proximity correction strategy. The data collected in the LETI pilot line environment provides a first extensive overview on the maturity degree of this low energy accelerating voltage option to meet industry requirements in the 2015 horizon.

2. ENVIRONMENT OF IMAGINE PROGRAM

2.1 Short focus on IMAGINE program objectives and partnership

The LETI-MAPPER IMAGINE program opened to industry partners intends to develop the required infrastructure to secure the quick start-up of the multi beam technology, as summarized in figure 1. It received the strong support of two major IC manufacturers STMicroelectronics and TSMC. Moreover, as detailed in figure 2, this initiative relies on a strong and growing partnership of large infrastructure partners working together with MAPPER and LETI in all the key fields of the technology from resist process to data handling.

- **Assess the capability of MAPPER technology**
- **Assess MAPPER technology against end users requirements**
- **Develop and provide the necessary infrastructure**
  - Process
  - Data flow
  - Proximity Effect Correction
- **Develop the applicability for 2 priority markets**
  - Semiconductor Manufacturing
  - Mask Making
- **Provide a competitive advantage to IMAGINE partners**

Figure 1 : Key missions of IMAGINE

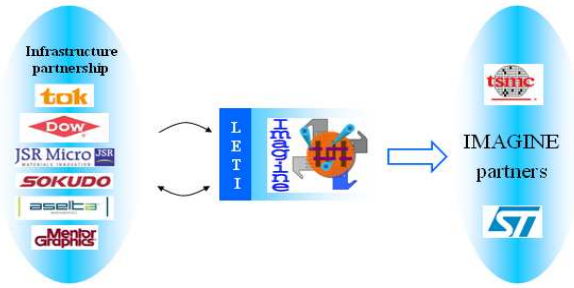


Figure 2 : Partnership status February 2011

2.2 Process infrastructure environment overview

All the work presented in this paper has been performed within the CEA-LETI 300mm pilot line facilities. On the process side, a SOKUDO RF^3 track has been used for coating, baking and development processes. For high quality coating, automated small dispense units were used to ensure a good resist film uniformity. Up to 20 different chemically amplified resist (CAR) formulations provided by the 3 resist partners have been evaluated during the last semester of 2010. To cope with the low penetration depth of 5keV electrons, film thickness was set at 50nm. For the tool start-up, HSQ was used as reference resist until a first mature CAR resist was available. All metrology operations were performed on a HITACHI CG4000 scanning electron microscope. The beam-to-beam measurement studies presented below have been performed on beams randomly chosen over the 110 operational beams of the pre-alpha platform.

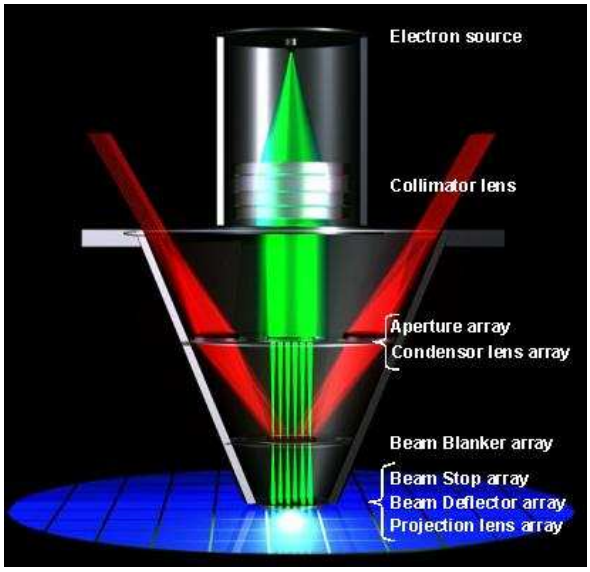


Figure 3 : Overview of the MAPPER technology

Key numbers 32nm node:	
	pre-alpha
#beams and data channels	110
Spotsize:	35 nm
Beam current:	0.3 nA
Datarate/channel	20 MHz
Acceleration voltage	5 kV
Nominal dose	30 $\mu C/cm^2$
Throughput @ nominal dose	0.002 wph
Pixel size @ nominal dose	2.25 nm
Wafer movement	Static

Figure 4 : Key characteristics of the Pre-alpha tool

The 300mm MAPPER platform is fully automated and the key characteristics of the pre-alpha platform installed at LETI are summarized above. 110 beams accelerated at 5keV are generated through the aperture array. From this MEMS essential element, beams are going through the beam blanker array. and at this level, the 110 beams are switched on and off individually by light signals, one for each e-beam. The beams control is generated through the data handling system containing the chip design in a bitmap format. Finally the beams are imaged at the wafer level through the last projection optic system. Beams issued from the blanker are going through or stopped at the beam stop array, then deflected and finally demagnified. The projection optic element was initially delivered with 35nm spot size capability and consequently upgraded current 2010 to 25nm spot size.

3. RESULTS AND DISCUSSIONS

3.1 MAPPER platform reliability

One first concern regarding tool performance is its overall reliability and repeatability. The tool stabilization in the LETI environment was one of the first priority. A weekly monitoring of the platform was set up on the key parameters. One important component of this follow-up operation was the source. Indeed any drift in the source will induce loss of dose control and beam position errors. Therefore, at wafer level, Critical Dimension (CD), CD uniformity (CDU) and beam position will not be controlled. A specific source monitoring has been installed and the figure 5 presents the evolution of source current emission versus applied tension at cathode level for a 3 month period. Source operating point is located in the flat region and this graph clearly shows the source aging process. When the operating point starts to drift into the slope area the dose control cannot be maintained thus leading to process fluctuations. This simple follow-up is helpful to determine the source lifetime and was very useful for the definition of a preventive maintenance program. Source is now replaced on a quarterly basis and this control procedure allowed to work under very control and stable conditions. Activities of the IMAGINE program could be performed in good conditions and during the second semester of 2010, more than 500 hours of exposure were realized with 75% of these exposures successfully completed, as summarized in figure 6.

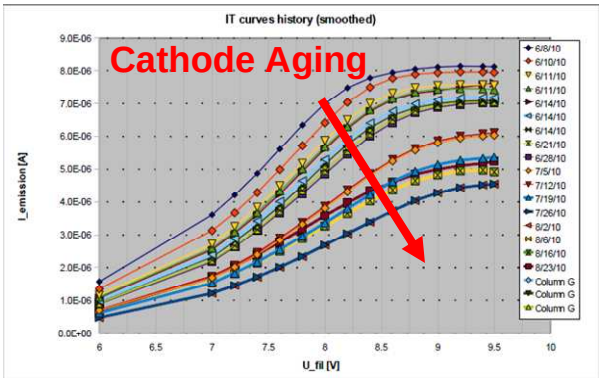


Figure 5 : Beam current emission versus tension at cathode level
Overview of 3 month follow-up

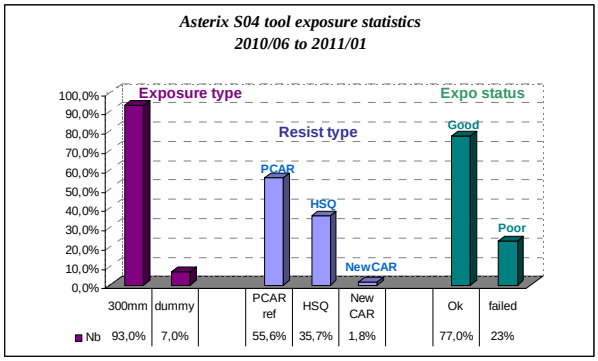


Figure 6 : Summary of LETI MAPPER pre-alpha tool usage

3.2 Tool ramp-up at LETI site

3.2.1 Phase 1 : Imaging performance at 45nm hp node

Once control of the key tool parameters was reached, the technology assessment program was initiated. It is structured in different phases linked to the pre-alpha configuration and upgrades plan. Beginning 2010, the MAPPER platform was delivered with a 35nm projection optics and without the blanker array. The resolution performances were targeted at 45nm half pitch (hp). Figures 7 and 8 presents the lithography results obtained in this configuration. As no CAR platform was yet available, this milestone was reached using HSQ resist. Tool imaging performances were measured on 20 beams randomly selected over the 110 beams available. It has to be noted that HSQ resist sensitivity is around 95µC/cm² at 5 kV, i.e. approximately seven times faster than at 50keV.

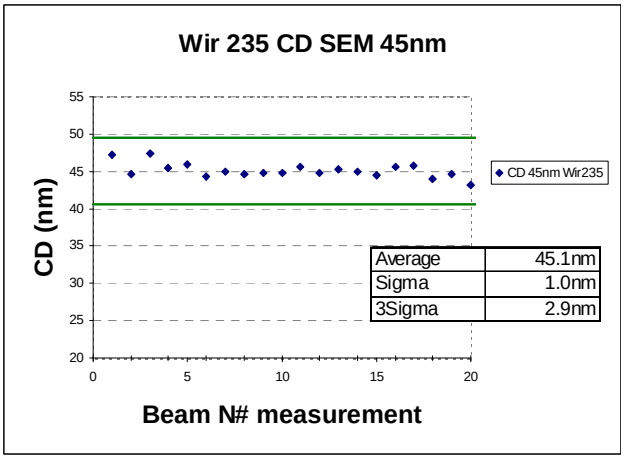


Figure 7 : Beam to beam CDU at 45nm hp

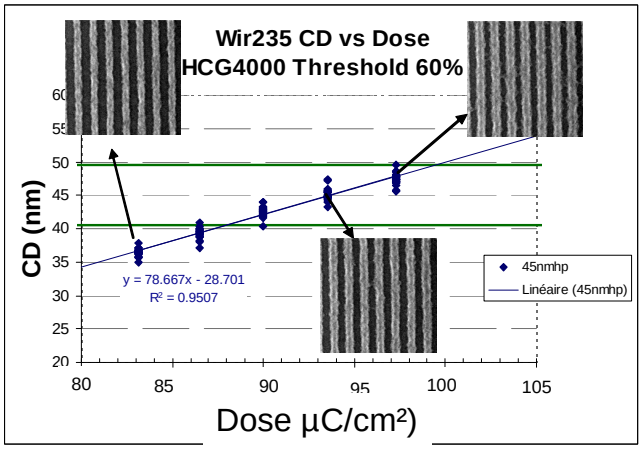


Figure 8 : Dose latitude at 45nm hp
HSQ resist – 50nm film thickness

3.2.2 Phase 2 : Imaging performance at 32nm hp node

After a stabilization period of the pre-alpha platform at this level of performances, it was decided to push the resolution by implementing a new generation of projection optics with a 25nm spot size capability. In parallel to this qualification work, a first positive CAR platform showed successful imaging performances, as described in the paragraph 3.3. This process became then our reference for the continuation of the tool assessment program.

The Figure 9 presents the dose latitude and CDU data summary for one wafer exposure. CD and CDU were within the targets: 32nm +/-10%. Dose to size is around 30µC/cm², sensitivity aligned with the final sensitivity target of the MAPPER platform for the development of a 10 wafers per hour machine. Figure 10 details the wafer-to-wafer repeatability over a 6 week period. Overall CD and CDU were in target showing a good repeatability of the pre-alpha tool. During this experiment, several resist batches have been employed and the exposure dose of the last batch was slower compared to the 2 previous ones.

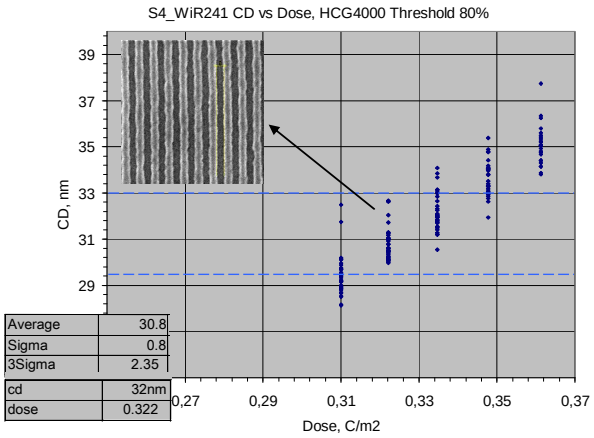


Figure 9 : Dose latitude at 32nm L/S Positive CAR resist – 50nm film thickness

		Dose2size 32nm hp (µC/cm²)	Average 31.2nm
Resist Batch 1	Wir191 BIAS	51.90	30.27
	Wir192 BIAS	48.50	32.54
Resist Batch 2	Wir205 BIAS	51.20	30.19
	Wir206 BIAS	52.50	28.45
Resist Batch 3 New MILO	Wir241 BIAS	33.30	31.97
	Wir242 BIAS	33.30	33.50

Figure 10 : Wafer to wafer reproducibility 32nm hp

3.2.3 Phase 3 : Imaging performance at 32nm hp node with beam blanker

After the successful implementation of the 25nm spot size upgrade, it was decided to integrate in the pre-alpha the beam blanker plate which allowed each beam to be driven individually. Figure 11 details beam to beam CDU for the exposure 267. It can be noticed that this new element did not affect the machine performances. Exposure latitude, presented in figure 12 for the exposure 266, remains unchanged with a large value and exposure dose stays around 30µC/cm². If we compare these 2 successive exposures it can be noticed that wafer-to-wafer repeatability is still within the +/-10% specifications. The pre-alpha machine at LETI will stay in this configuration until the start of a new upgrade phases scheduled current 2011.

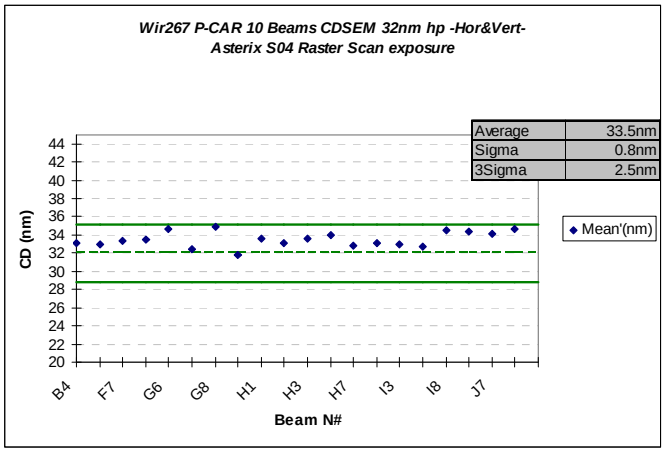


Figure 11 : Beam to beam CDU at 32nm hp
With blanker

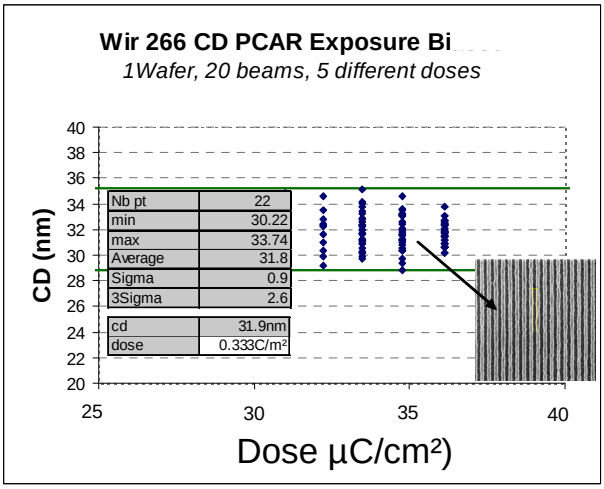
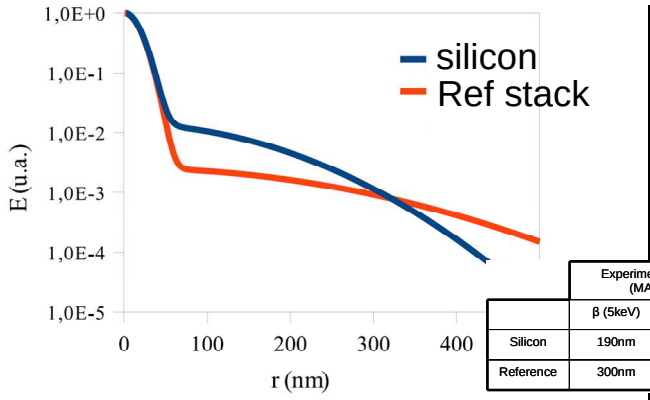


Figure 12 : Exposure dose latitude at 32nm hp
Positive CAR resist – Film thickness 50nm

3.3 Resist process development

3.3.1 Imaging stack adaptation

Resists for direct write lithography are widely commercially available but most of those platforms have been developed for 50kV accelerating voltage. At 5kV, which is the working condition of the MAPPER platform, overall know-how is less important. The composition of the imaging stack has to be optimized to deal with the specificity of the low accelerating voltage. The penetration depth of low energy electrons is much smaller as well as backscattered effects that are approximately 100 times lower than the 50kV one's. This stack has also to be compatible with the industry in terms of material and etching performances…



	Experimental Results (MAPPER)	
	β (5keV)	η (5keV)
Silicon	190nm	0,9
Reference	300nm	0,4

Figure 13 : Influence of process stack on point spread function

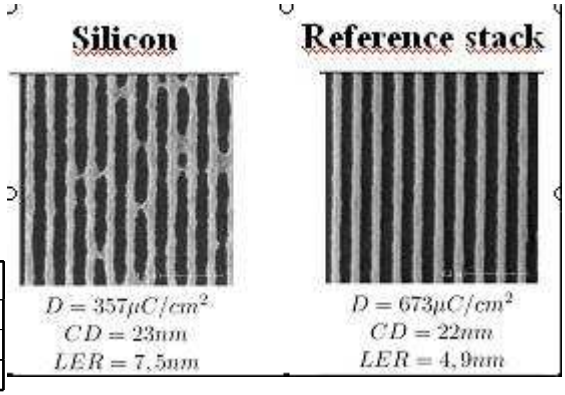


Figure 14 : Imaging performance of HSQ on silicon and reference stack

To deal with low penetration depth and keep a straight resist profile, the film thickness has to be reduced around 50nm, which is similar to the film thickness that will be used for extreme ultra violet (EUV) lithography. On the other hand the imaging contrast can be increased through process stack optimization by reducing the overall backscattered effects. Figure 13 presents the resist point spread function on bare silicon and using our reference process stack. As it can be noticed the, overall background represented by the η parameter (ratio between forward and backscattered electrons) is significantly smaller (X2). The impact on imaging performance is directly visible in figure 14 on the HSQ lines resolved on silicon and on this reference process stack. All the imaging results presented in this paper have been obtained on this specific stack.

3.3.2 Outlook on Chemically amplified resist imaging performance

Another important part of the IMAGINE program is the development and qualification of resist platforms optimized for 5kV accelerating voltage technology. Up to 20 different CAR platforms were evaluated during 2010 last six months. The first objective of IMAGINE was to qualify a first CAR platform compatible with CMOS environment and aligned with the 32nm hp resolution target, .obtained results are highlighted in figure 15. This resist formulation is now used for the tool follow-up and is our reference material for the benchmark activities. Furthermore this platform shows a sensibility level around 30µC/cm² aligned with the throughput target (10wph) of the MAPPER technology high volume manufacturing platform. Finally this resist even demonstrated a resolution capability down to 27nm L/S with high patterning quality

Different resist formulations have been screened and a snapshot of the results obtained on both positive and negative tones is presented in the figures 14 and 15. On the positive CAR side, fast resist platform, around 10µC/cm², with resolution down to 40nm hp will be an interesting material for high throughput applications allowing significant writing time gain for either relaxed technology nodes or non critical layers.

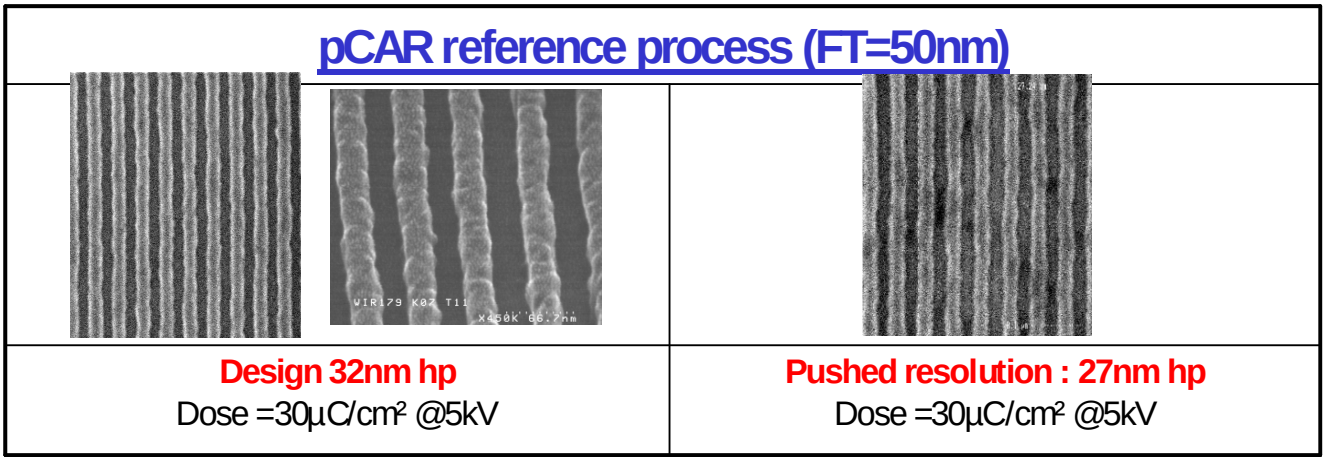


Figure 13 : Overview of CAR reference process capability for L/S patterning

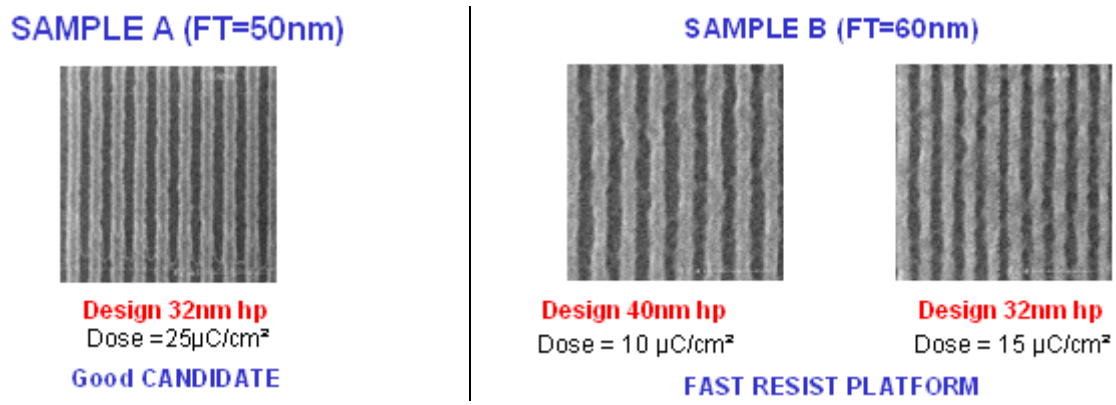


Figure 14 : Example of pCAR resist formulation tested on MAPPER platform at 5kV

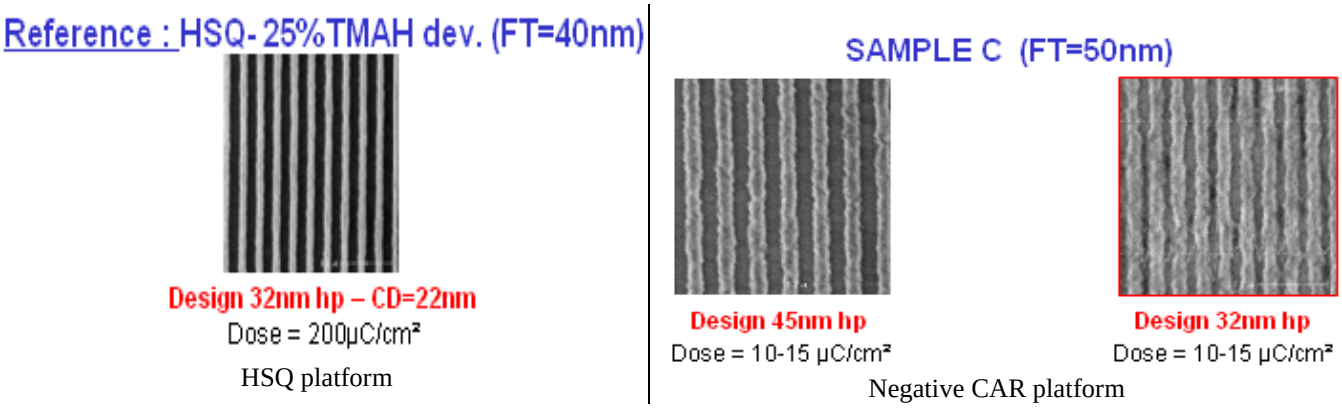


Figure 15 : Resolution achievement on negative tone resist

For the negative tone resist, HSQ platform gives currently the best performances on the MAPPER tool with 22nm features printed. Resolution and roughness can be improved on this resist by using more aggressive TMAH developer normality at the expense of increasing significantly the exposure dose (factor of 2). Concerning negative CAR platform, development is today unfortunately poorly supported by resist suppliers and should require more attention. Indeed such negative tone resists would have a great impact in minimizing backscattered contribution for the patterning of clear field levels. 45nm hp represents up to now the best resolution achieved so far.

3.3.3 First process integration demonstration

Figure 16 and 17 details the integration tests performed on both HSQ and positive CAR resists. The first purpose was to demonstrate that aggressive patterns can be transferred into the final technological stack. This work demonstrated that no major issues are foreseen and confirmed that resist process developed on and for low accelerating voltage are fully compatible with the standard CMOS flow.

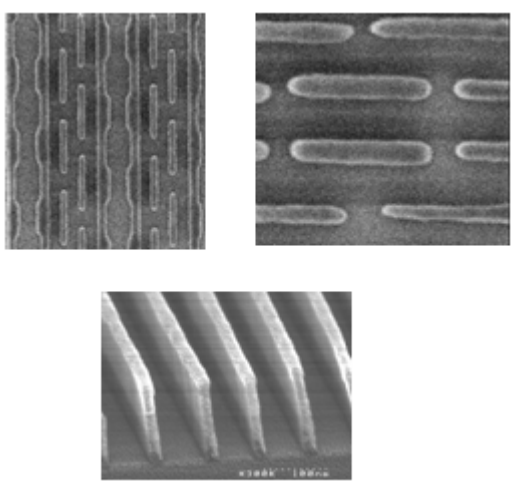


Figure 16 : Etch transfer study of 22nm logic gate HSQ resist – 22nm CD

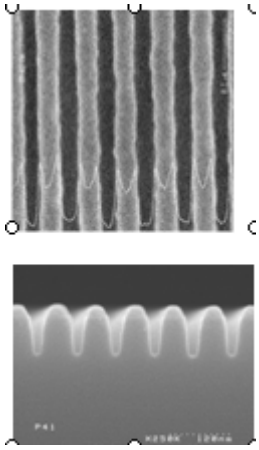


Figure 17 : Etch transfer study of positive CAR Reference process – 32nm hp

3.4 Quick snapshot on E-Beam proximity correction

Another important element for maskless lithography toward a high volume manufacturing platform will be its data path infrastructure. This thematic covers a wide range of activities. The first part has to be performed off-line and includes all data treatment from the GDS file to the final format, i.e. fracturing, implementation of proximity correction and final input format. The second phase will be performed in line with tool specific inputs like, for example, beam position correction.. One goal of IMAGINE is to define the specifications of this future infrastructure. As shown for example in figure 18, in the case of the implementation of the proximity corrections, the work performed intends to determine what is the best strategy between the standard dose modulation applied today in E-beam lithography or alternative approaches OPC-like strategy based on geometry correction only or a combination of both solutions. Several works are initiated to understand the sensitivity and accuracy of each strategy as shown in figure 19 where the CD error of various 1D and 2D test structures is evaluated versus the proximity correction strategy[4].

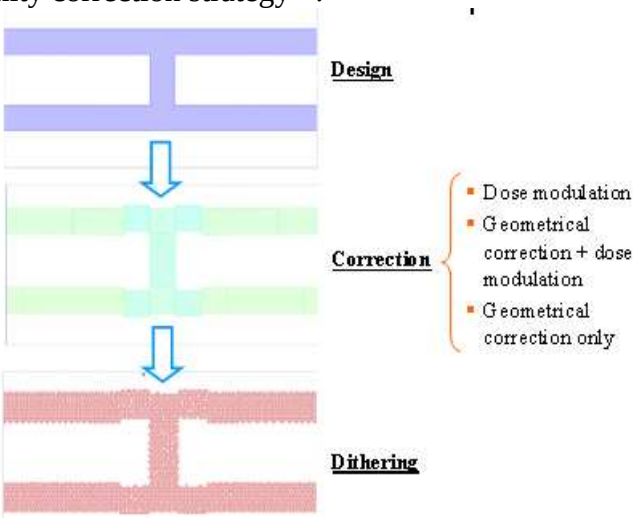


Figure 18 : Schematic of off-line data treatment for multibeam lithography

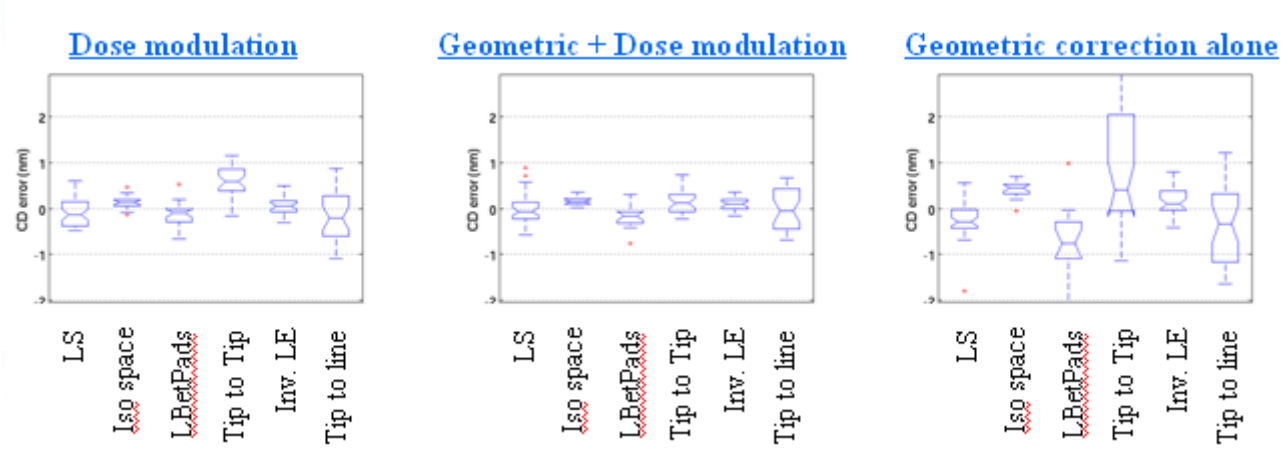


Figure 19 : Sensitivity of various 1D and 2D test structures versus proximity correction strategy

4. CONCLUSIONS

Significant achievements have been reached in 2010 within the IMAGINE program. After a first period dedicated to platform hardening, the ramp-up of the MAPPER pre-alpha platform within the LETI environment has been successfully performed according to its objectives. End of 2010, the tool is configured with the beam blanker element and can resolve 27nm hp features in positive tone chemically amplified resist. This achievement confirms the potential of this technology as a real option to address CMOS manufacturing. The IMAGINE program with its industrial partners will continue its assessment mission in 2011 and will pursue the qualification of the new planned upgrades on the LETI platform: beam to beam stitching, resolution improvement and alignment demonstration. It will intensify the development of its infrastructure to provide to its partners a competitive advantage ahead to the future insertion of this technology into an industrial environment.

5. REFERENCES

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