Machine Learning in Computational Lithography

Yu Cao

ASML-Brion

San Jose, February 2019

This is really a no-brainer …

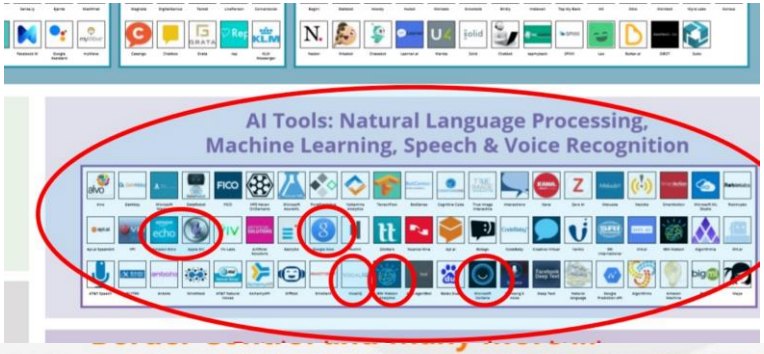

G Dan Hutcheson

What's Happening and *What's the Meaning*:

ASML introduces AI to its product portfolio: *This is really a no-brainer. That said, the problem that most equipment companies have is finding good applications for it, as they find all they have is little data to feed the NN (more on that below). Anyway, this will be a good test for DLNNs as to whether engineers will accept results without knowing what's in the 'blackbox,' which is a classic barrier to this technology. I believe they will because comparing results to input consistency are pretty easy to test out in this case. Especially since ASML led the way into computational lithography, albeit with plenty of customer pull.*

Source: ***The Chip Insider®*** VLSIresearch

Machine learning brings revolution to many applications!



AlphaGo

Can machine learning be the moonshot for us?


Security & Counterterrorism: Fighting


Security & Counterterrorism: Chasing

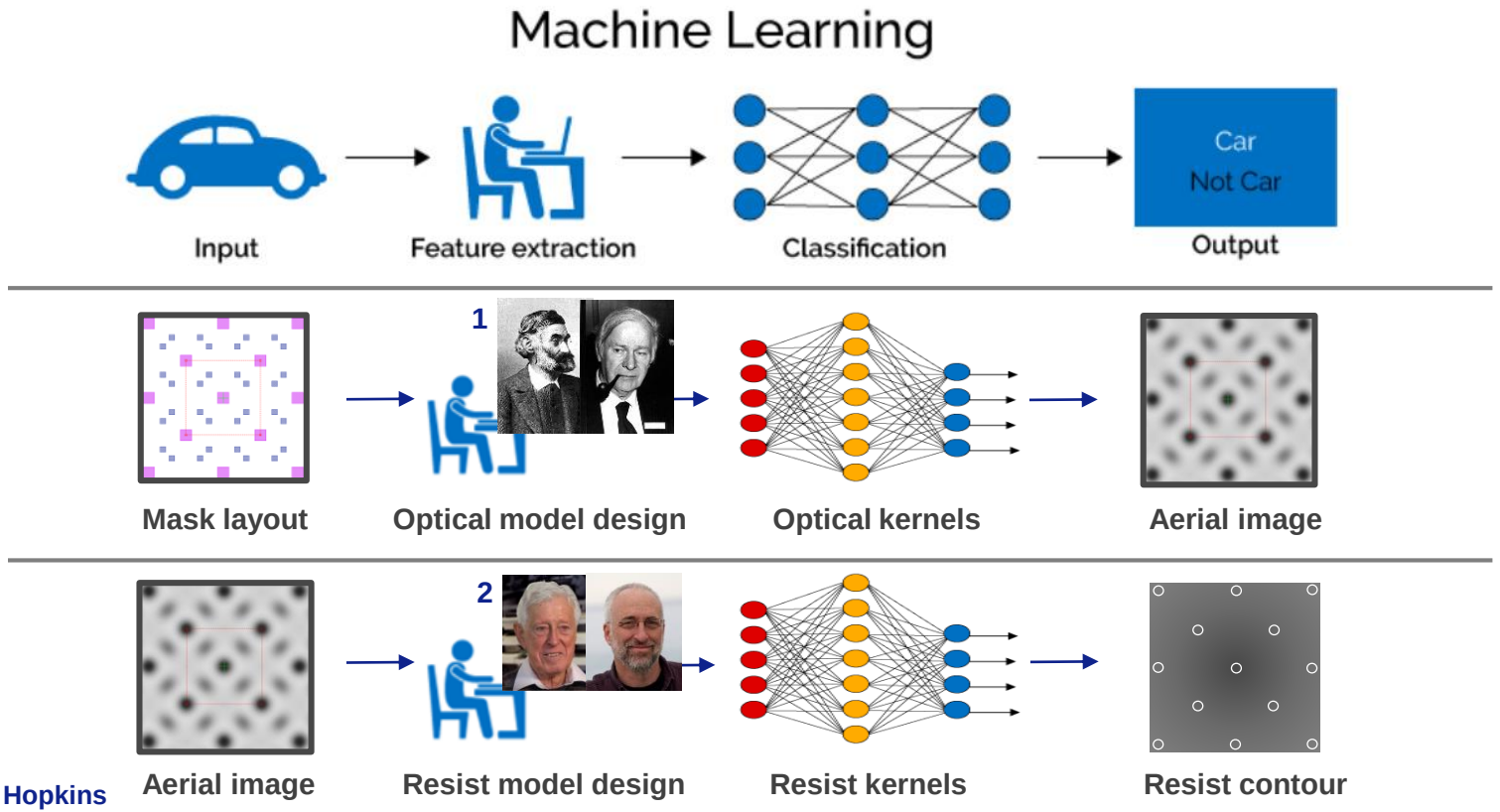

Banking: ATM Protection


Rail: Driver Fatigue


Mining: Production Safety


Intruder Alerts

We have been doing machine learning for a long time …
with manual feature engineering

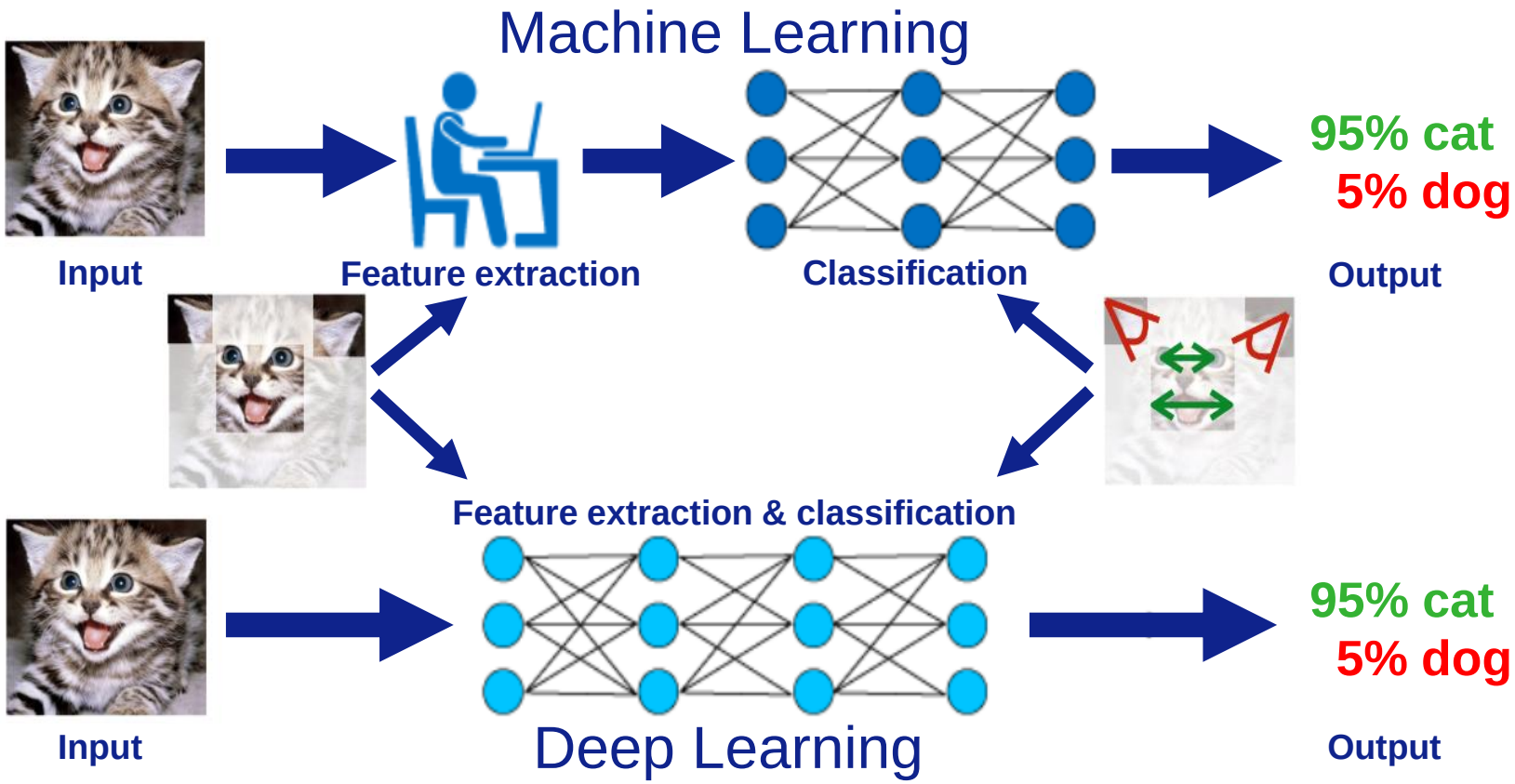


1: E. Abbe, H. H. Hopkins

2: F. H. Dill, C. Mack

Machine Learning evolved to Deep Learning

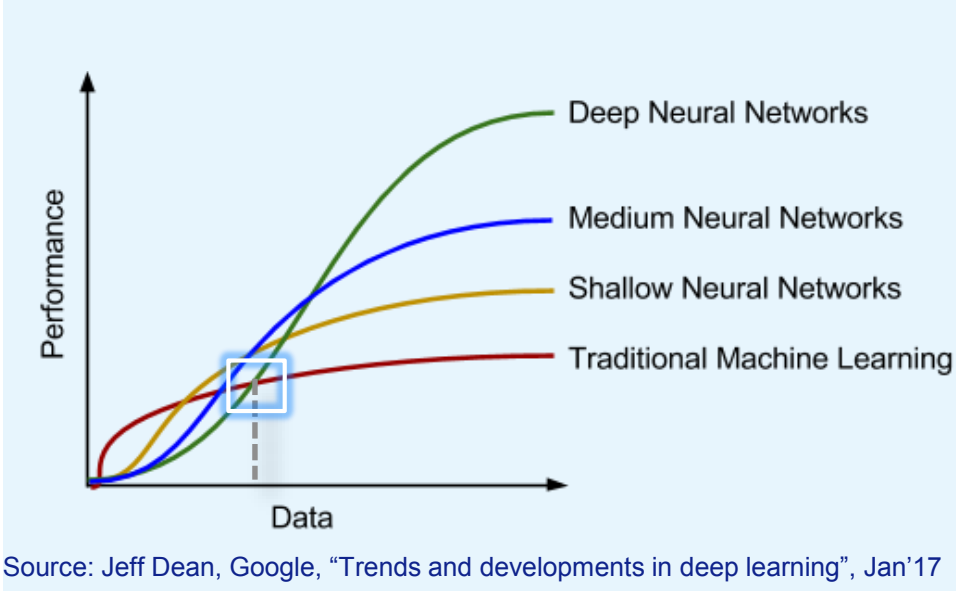
Less human intervention in growing data volume analysis



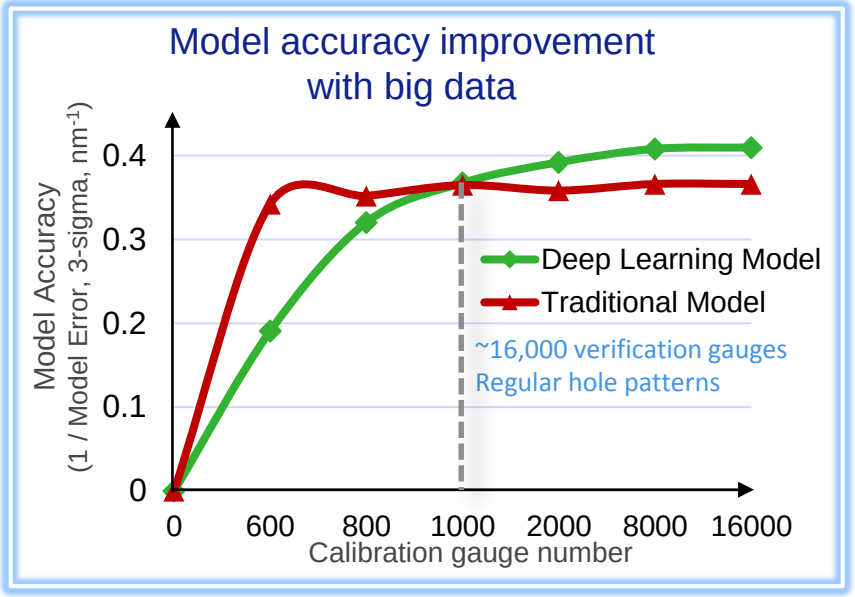
Based on: Jagreet Kaur Gill, “Log Analytics With Deep Learning And Machine Learning” April 28, 2017

Massive metrology data & deep learning models further improve OPC accuracy in customer case

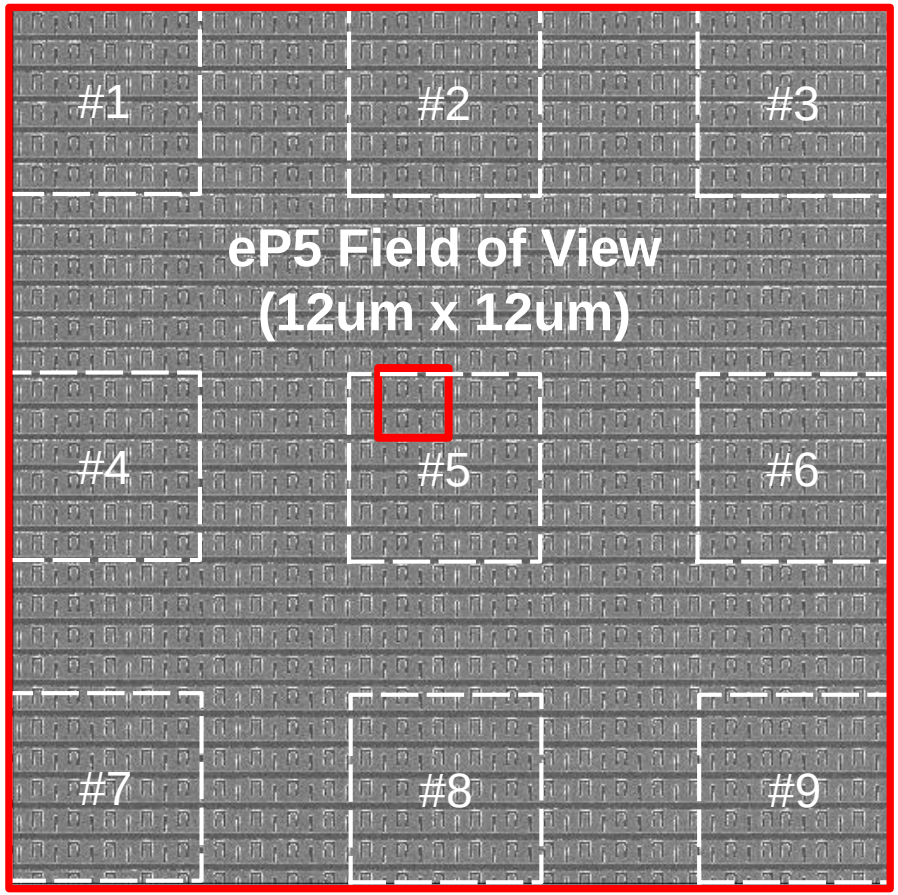
- Big data improve pattern coverage & enhance model accuracy
- Deep Learning Model has more benefits with big data vs Traditional Model



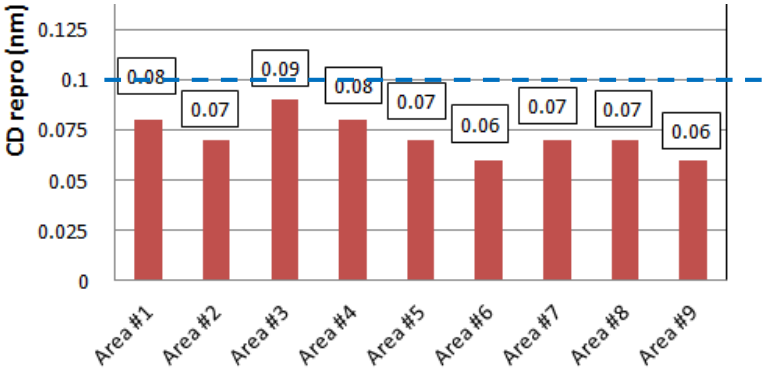
Source: Jeff Dean, Google, “Trends and developments in deep learning”, Jan’17



High speed e-beam metrology and large field of view

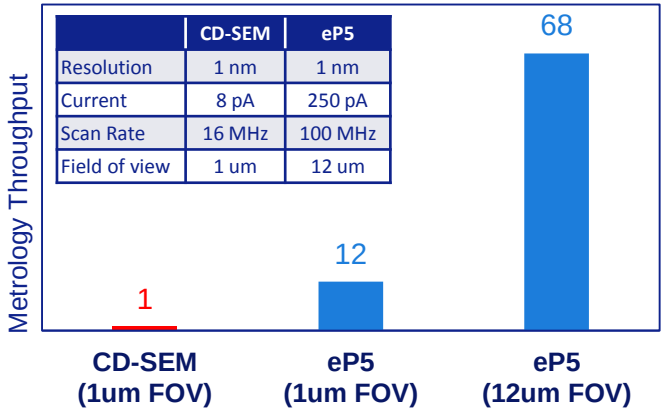


Excellent precision across large field of view



Throughput advantage over CD-SEM

	CD-SEM	eP5
Resolution	1 nm	1 nm
Current	8 pA	250 pA
Scan Rate	16 MHz	100 MHz
Field of view	1 um	12 um

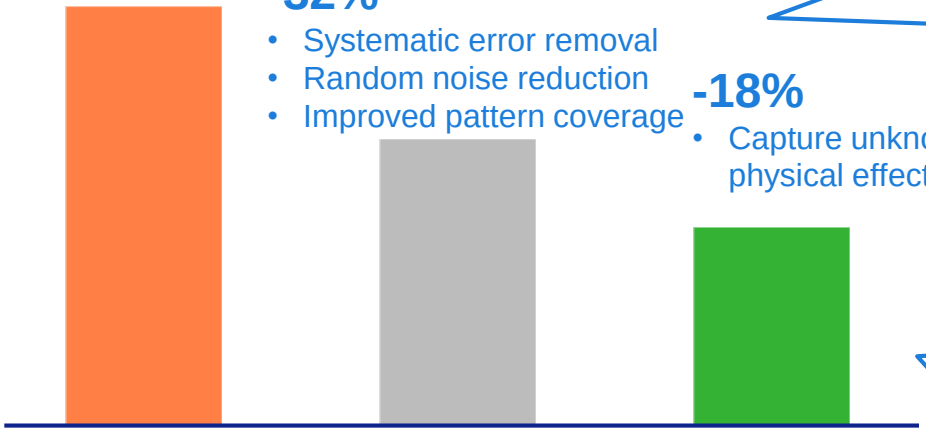


Improving OPC model accuracy by 2X on DRAM

enabled by deep learning, fast e-beam, and metrology processing

Model prediction error (RMS)

validated with >150k Edge Placement (EP) Gauges



-32%

- Systematic error removal
- Random noise reduction
- Improved pattern coverage

-18%

- Capture unknown physical effects

Baseline metrology w/o deep learning (CD gauges)

~18 hours

Metrology collection time

eP5-MXP w/o deep learning

3.3x (CD+EP gauges)

eP5-MXP with deep learning

3.3x (CD+EP gauges)

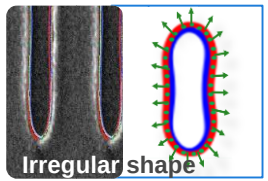
~3 hours

Metrology collection time

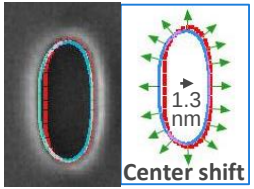
3x images

eP5-MXP metrology

Improving 2D metrology accuracy with contour based measurement



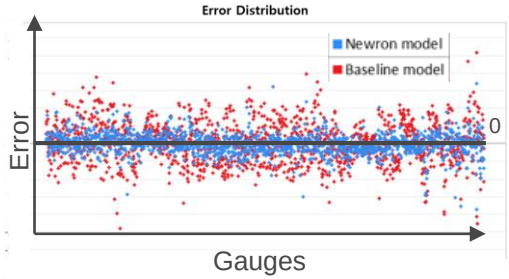
Systematic error reduction without **shape fitting**



EP gauges capture **pattern shift**

Deep learning resist model

Improve OPC model accuracy



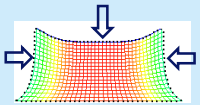
OPC Model accuracy study using high volume contour based gauges and deep learning on memory device, Young-Seok Kim et al., SPIE 2019, 10959-37

Better accuracy of lithography models by deep learning

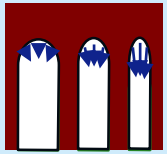
Enabled by fast e-beam metrology and physical based models

Stability

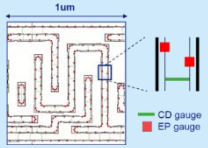
Physical driven **training** using physics based lithography models



Physical Resist Shrinkage



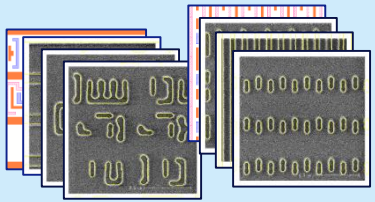
Resist surface stress



Data expansion through simulated contours

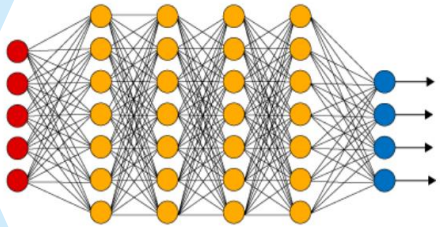
Accuracy

Data-driven **training** based on fitting spec and wafer measurements

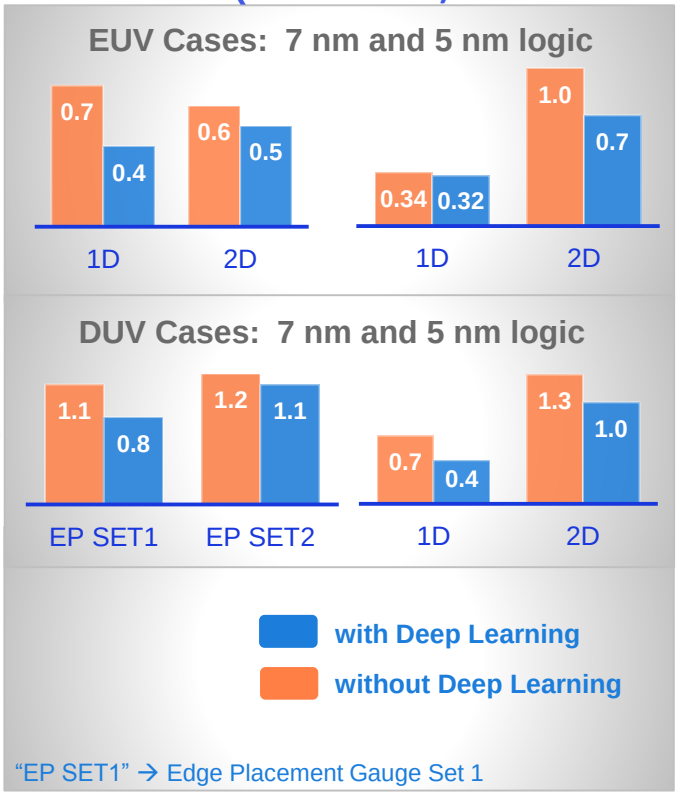


Large volume wafer metrology data, further enhanced by fast e-beam

ASML Deep Learning model



Model Prediction Accuracy (RMS in nm)

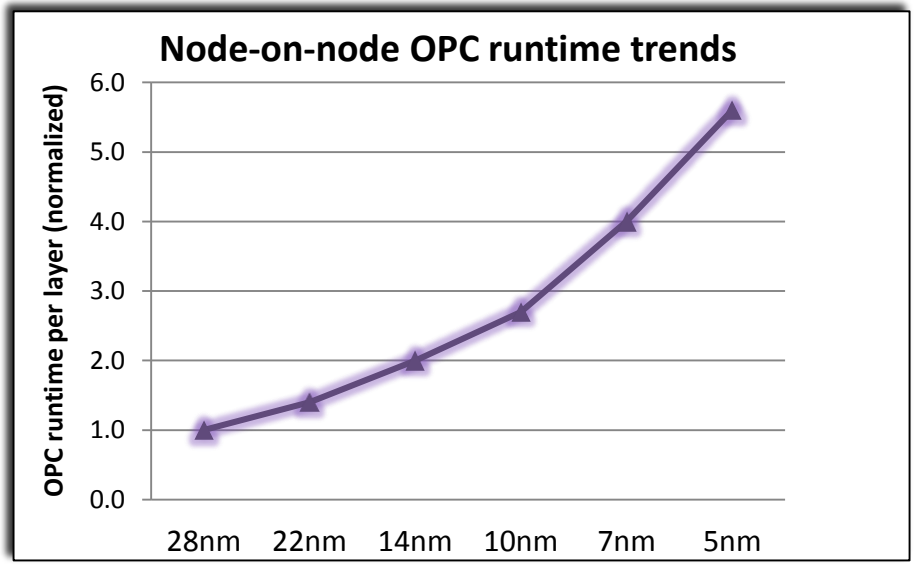


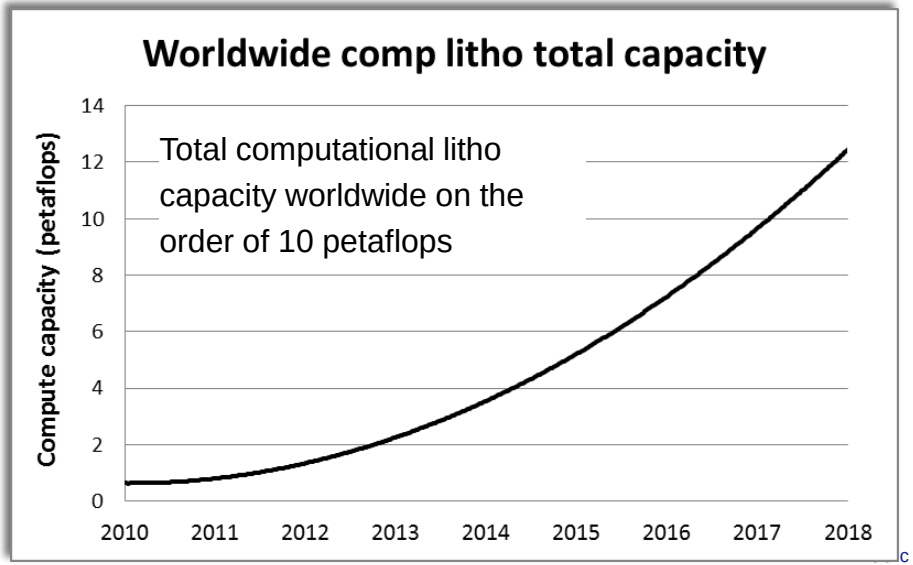
"EP SET1" → Edge Placement Gauge Set 1

“Moore’s Law” of Computational Lithography

Runtime and cost of OPC increases node-by-node

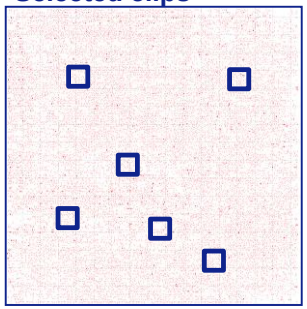
Technology Node	28nm	22nm	14nm	10nm	7nm	5nm
Production start	2011	2013	2014	2016	2017	2019
Average transistor density (billion/cm^2)	1.17	1.63	2.34	3.75	6.25	10.71
Number of critical layer masks	18	24	33	37	47	66
Normalized OPC runtime per layer per unit area	1	1.4	2	2.7	4	5.6





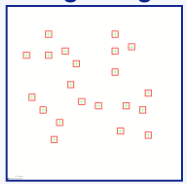
Deep learning inverse model speeds up full-chip OPC by providing a good starting point

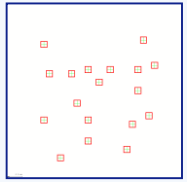
Selected clips



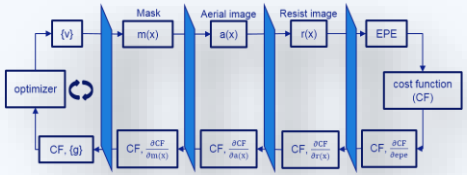
Training *on clips*

Design target



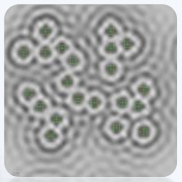


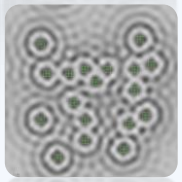
Training input



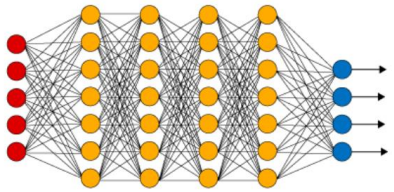
Complex, Iterative Optimization

Inverse mask image





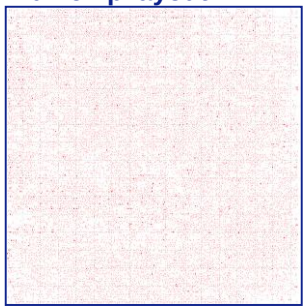
Training input



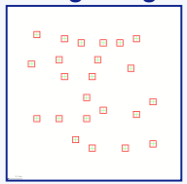
Deep Learning Inverse Model

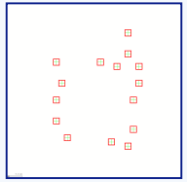
Inference *on full chip*

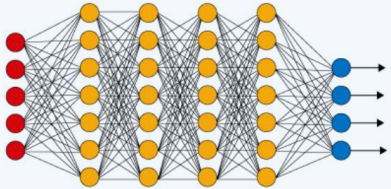
Full chip layout



Design target

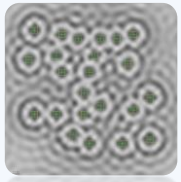


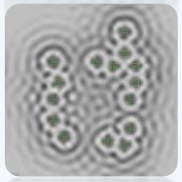




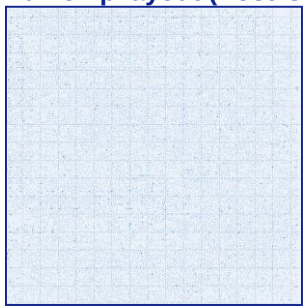
Deep Learning Inverse Model

Inverse mask image

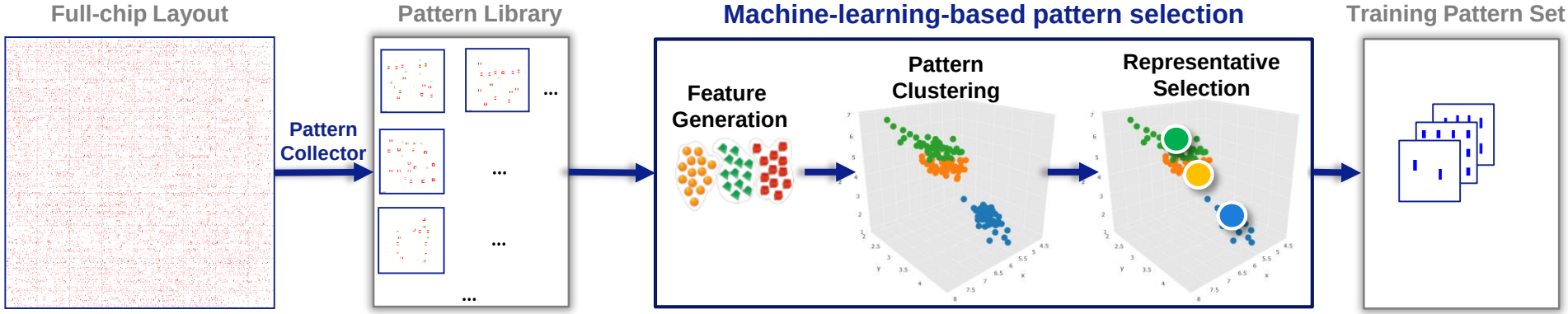




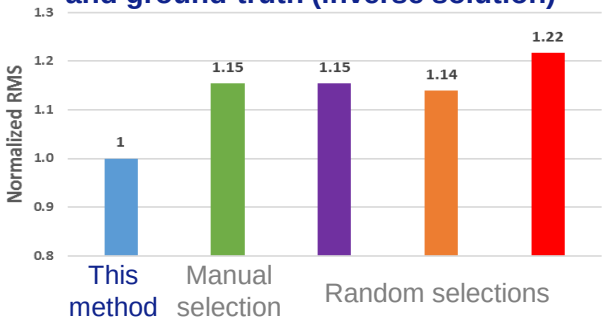
Full chip layout (Post-OPC)



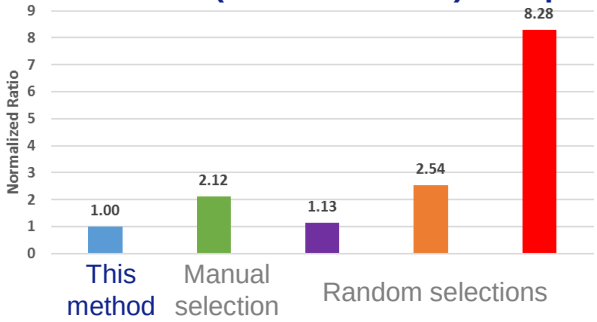
Improving training pattern coverage using machine-learning-based pattern selection



Normalized RMS between prediction and ground-truth (inverse solution)



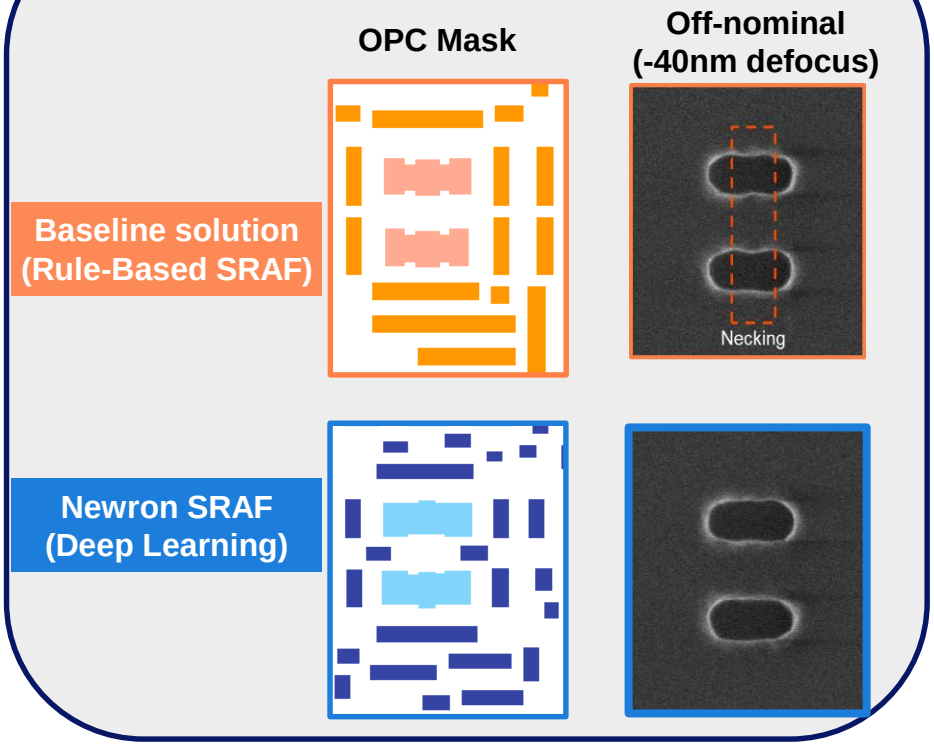
Critical PV-band (>15% CD error) Comparison



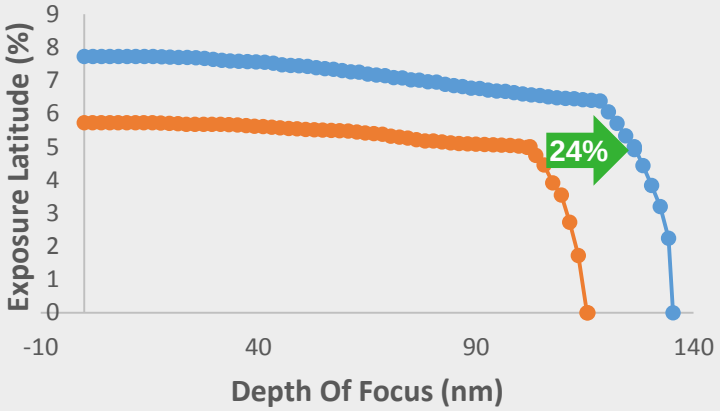
Full-chip application of machine learning SRAFs on DRAM case using auto pattern selection K. Chen et al., SPIE 2019, 10961-37

Deep learning SRAF improves full-chip DoF by 24% for DRAM contact hole layer, validated on wafer

Newron SRAF places more accurate assist features to remove the process window limiter



Newron SRAF wafer validation shows 24% DoF improvement



	Baseline (RB-SRAF)	Newron SRAF
DOF @ 5% EL	102 nm	126 nm

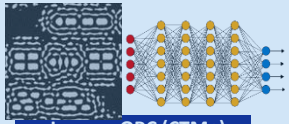
Full-chip application of machine learning SRAFs on DRAM case using auto pattern selection K. Chen et al., SPIE 2019, 10961-37

Leverage confluence of new technologies to meet OPC technology and cost requirements

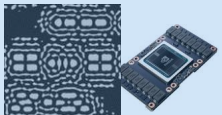
2016	2017	2018	2019	2020	2021

ASML

Inverse OPC (CTM)



Inverse OPC (CTM+) Deep Learning Inverse



Inverse with phase control Hardware Accel. (tentative)

intel

Skylake

Intel DL Boost

Cascade Lake

Cooper Lake

14 → 10 nm

Ice Lake

intel Nervana™

Spring Crest

NVIDIA

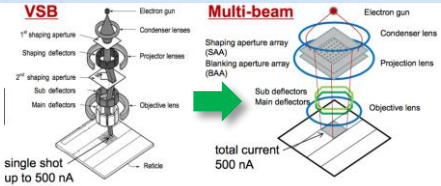
Pascal

Volta

Turing

Next Gen?

Mask writer & inspection

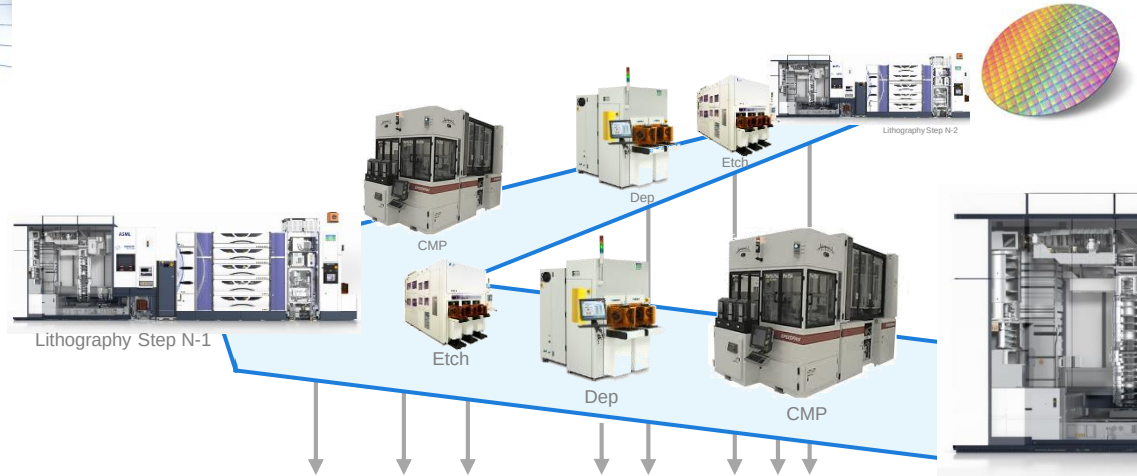


Multi-beam Mask Writer available

Mask inspection available

Mask making infrastructure is ready for inverse OPC & curvi-linear masks

Context-aware control extends holistic solutions



Context Data

Corrections

VCP
Virtual Computing Platform

Litho InSight and Pattern Fidelity Enhancements

Leveling, Alignment, Metrology Overlay, Focus, pattern defect control and scanner/etcher co-optimization

Metrology design & setup

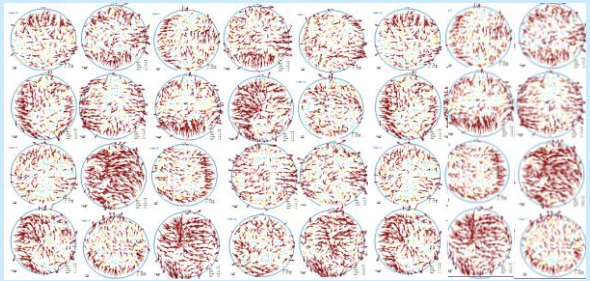
Model, sampling & control setup

Monitoring & analytics

Leverage machine learning to address wafer-to-wafer variation induced by different wafer process routes

Wafer to Wafer Variation

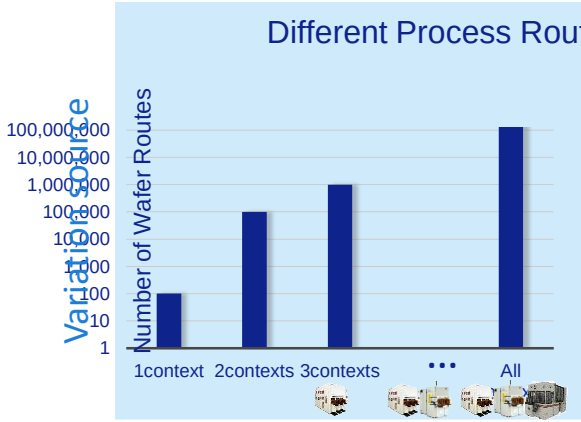
Overlay Variations



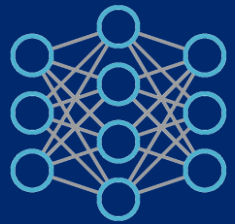
Every month > 100,000 wafers exposed per scanner

Variation source

Different Process Route

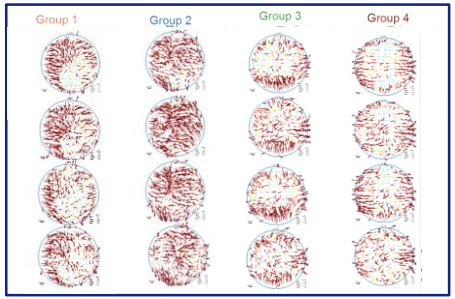


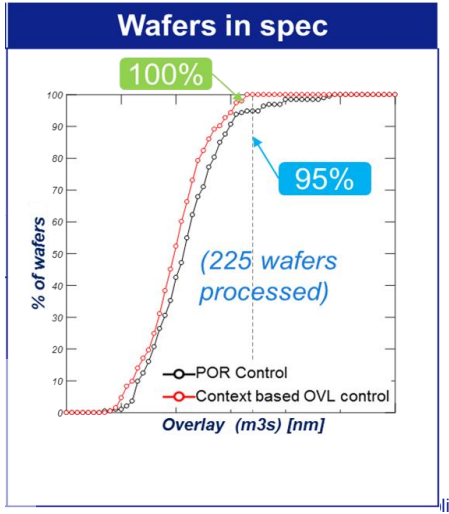
ASML Machine Learning Model



Correlate wafer-to-wafer variation to process context and apply run-to-run control with context-based grouping

Context based Overlay Control results





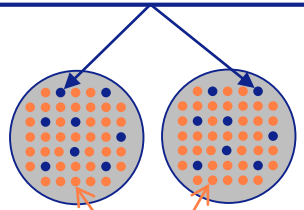
A novel patterning control strategy based on real-time fingerprint recognition and adaptive wafer level scanner optimization
H. E. Hakli et al., SPIE 2018, 10585:105851N

Predict dense alignment from dense leveling data hybrid metrology enabled by machine learning

Type 1

Known input

- Leveling & Alignment all wafers
- Overlay or alignment sampling from same wafer (blue points)



Prediction

Unknown (orange points)

- Overlay or alignment from same wafer at different coordinate locations

Machine Learning

Pairing wafer leveling metrology from a lithographic apparatus with deep learning to enable cost effective dense wafer alignment metrology

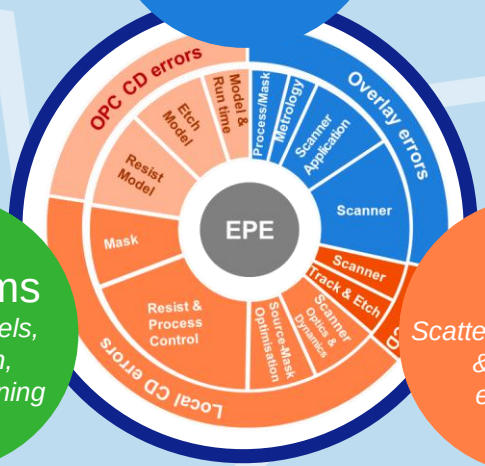
E. Schmitt-Weaver & K. Bhattacharyya, SPIE 2019, 10961-7

Holistic Lithography delivering significant customer value

Lithography scanner with advanced control capability

Etch and deposition tools

Applications
Patterning Control



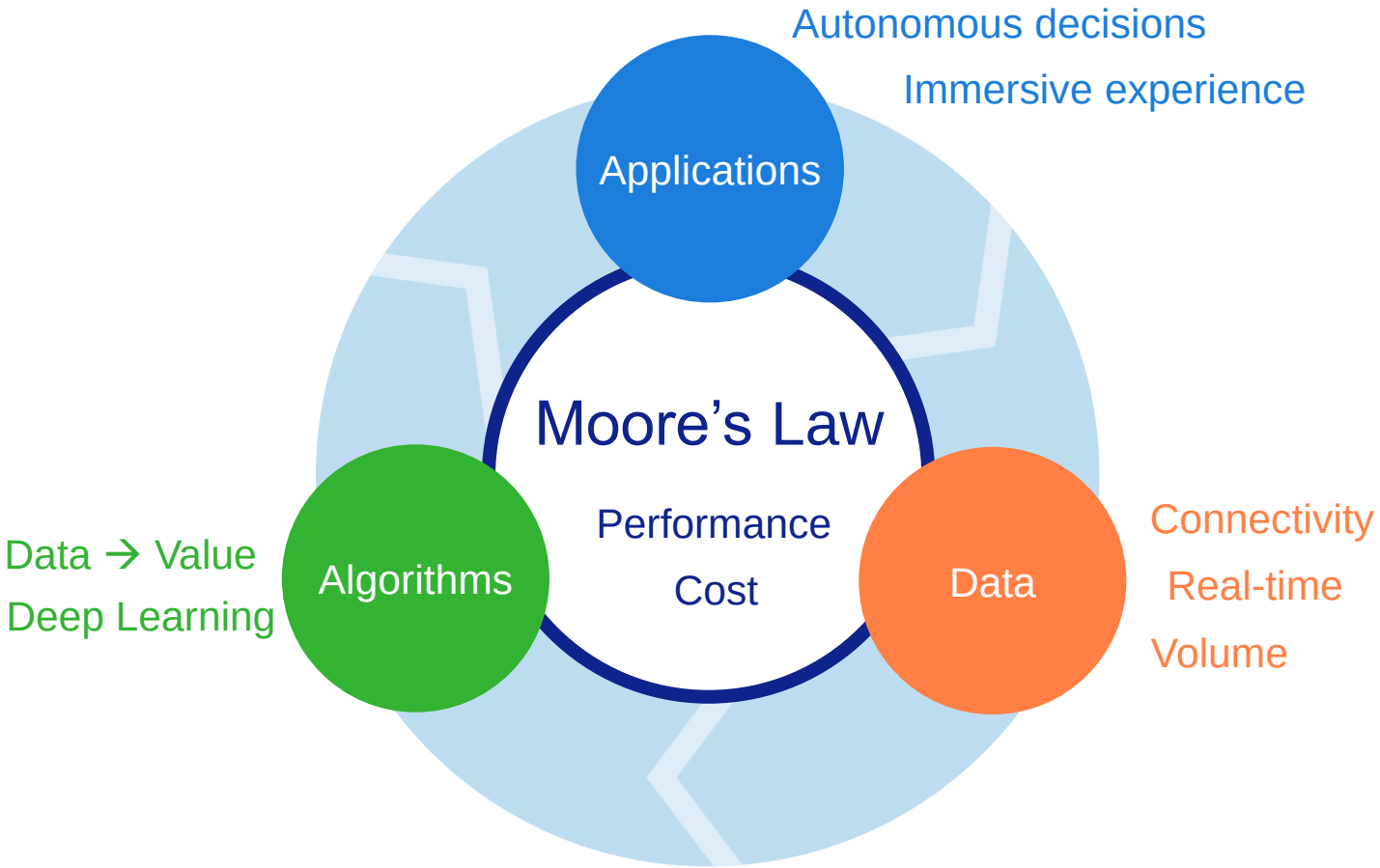
Algorithms
Physical Models, Optimization, Machine Learning

Data
Scatterometry, SEM, & other fab equipment

Computational lithography and metrology

Optical and e-beam metrology

Major trends in semiconductor-enabled computing



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