



Mask Metrology in the ILT World



Linyong (Leo) Pang

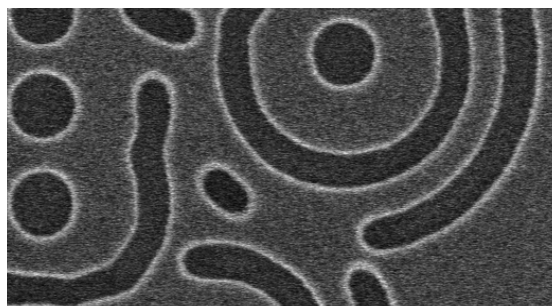
D2S, Inc.

Sept. 29, 2015

A Decade of ILT!



2005



6

Papers

2

Foundries

1

Memory

1

Mask shop

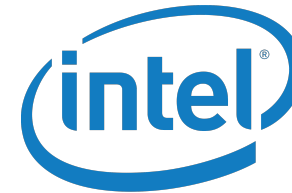


ILT Adopted as the Way Forward



>200

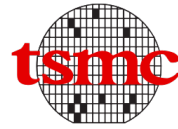
Papers



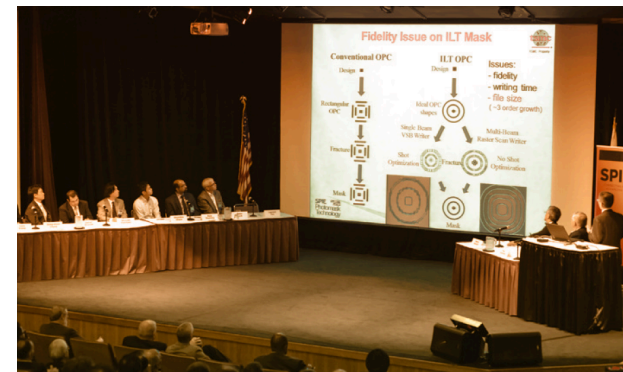
台灣積體電路製造股份有限公司
Taiwan Semiconductor Manufacturing Company, Ltd.

Officially
announced

Today



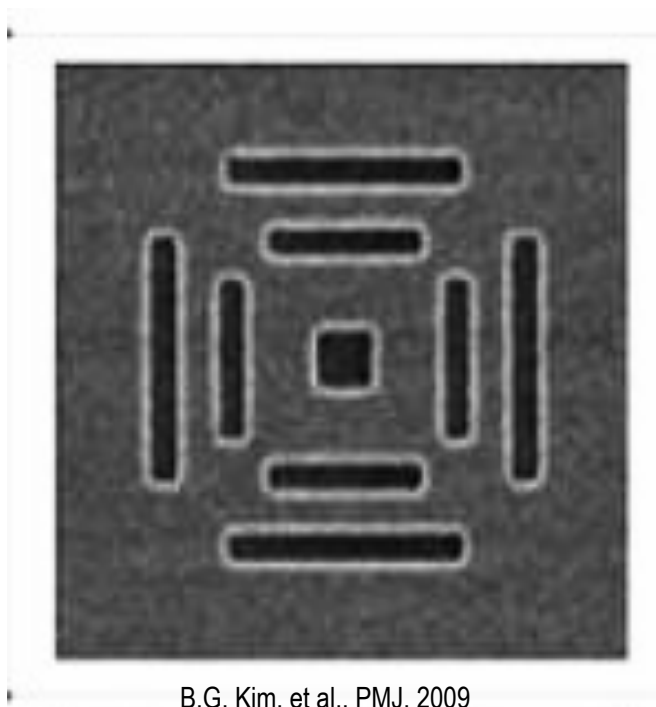
台灣積體電路製造股份有限公司
Taiwan Semiconductor Manufacturing Company, Ltd.



ILT expertise proliferated

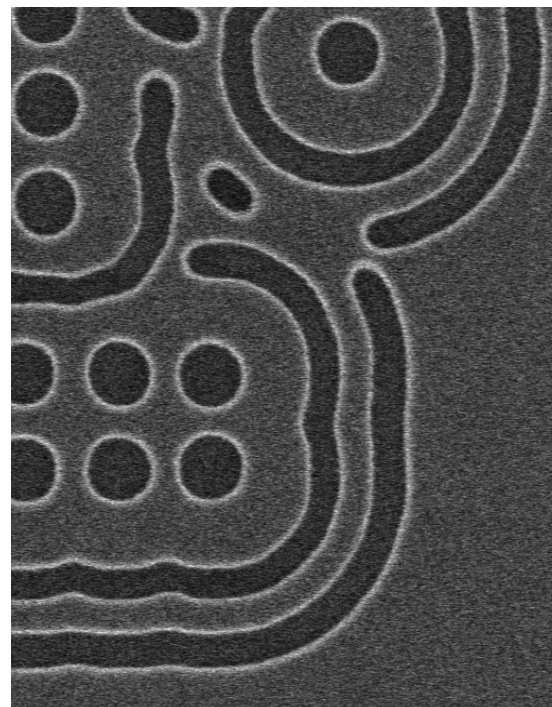
2014 panel

But What About CD Metrology?



B.G. Kim, et al., PMJ, 2009

VS



B.G. Kim, et al., BACUS, 2012

Old World:
Conventional
Mask Pattern

New World:
ILT Mask
Pattern

What *is* CD In the ILT World?

ILT CD is not just
line width: it's 2D!

Contour and EPE

What to use as a
reference?

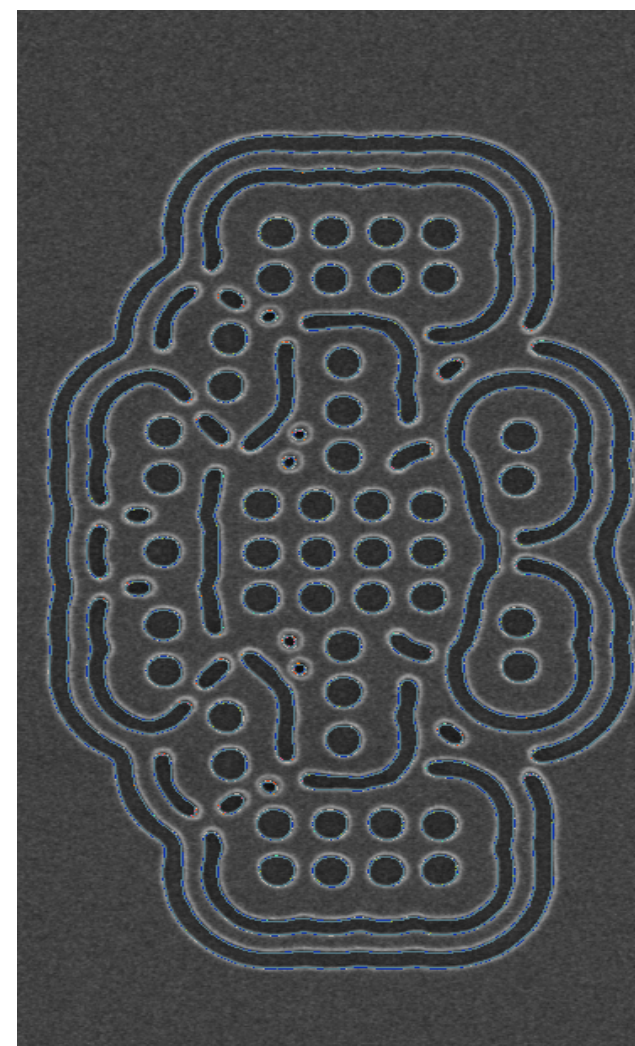
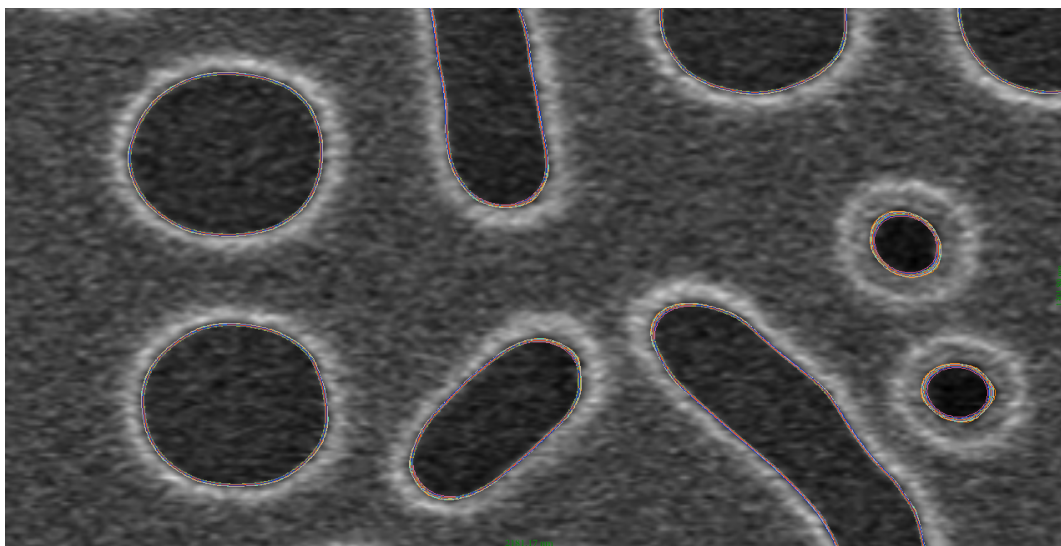
Simulated mask
pattern

Which mask issues
impact the wafer?

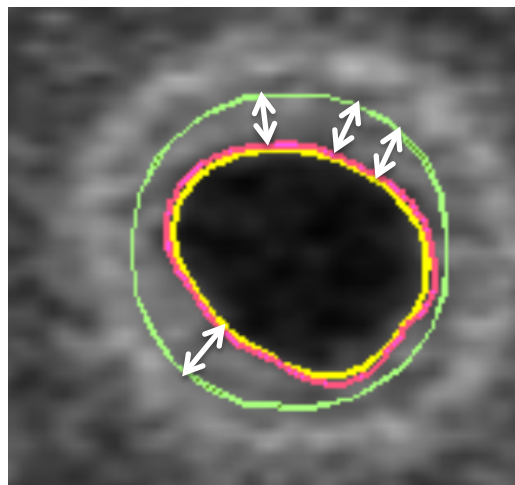
Wafer plane analysis

Mask Plane Metrology: Contour and EPE Measurements

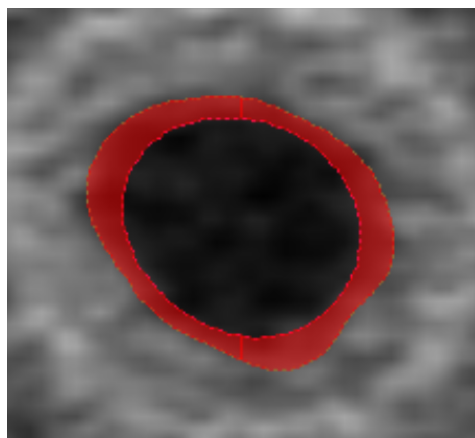
- EPE measured on entire contour
- Histogram: mean, 3 sigma



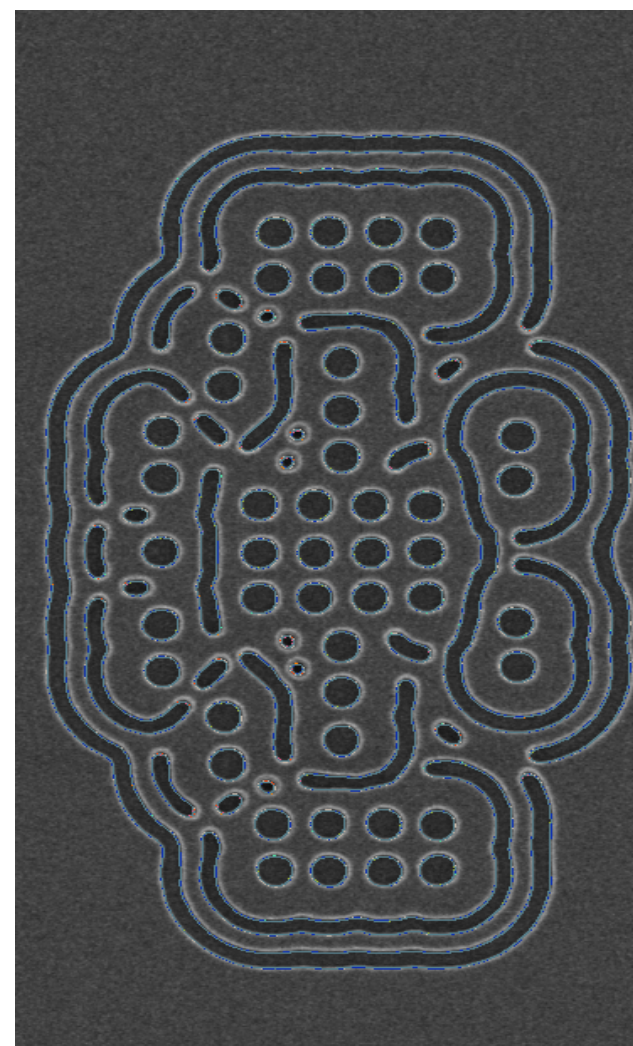
Mask Plane Metrology: Contour and EPE Measurements



EPE measured on
entire contour



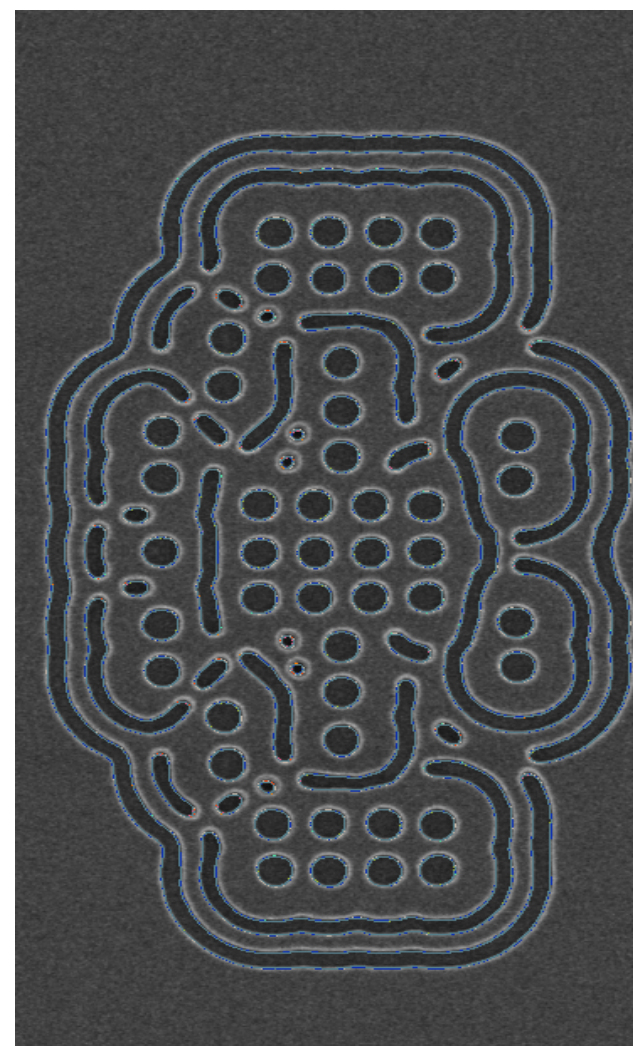
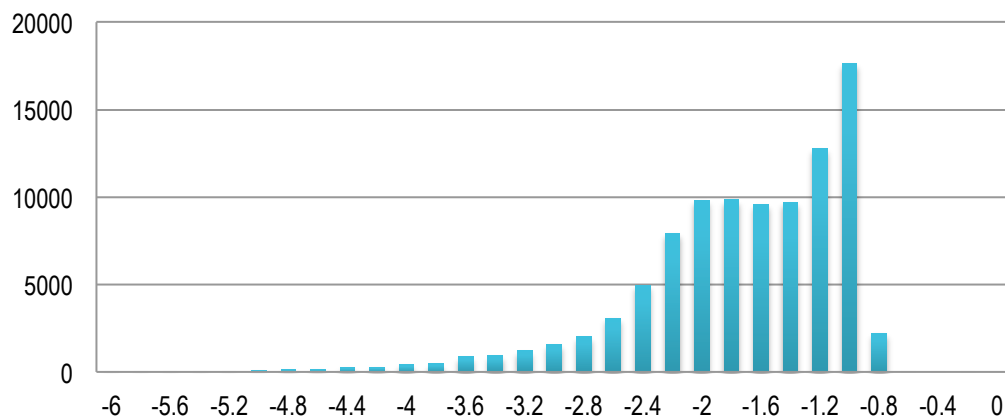
PV band



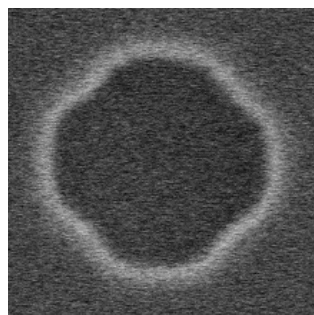
Mask Plane Metrology: Contour and EPE Measurements

Count	95883
Min (nm)	-6.00
Max (nm)	-0.84
Mean (nm)	-1.83
Median (nm)	-1.71
3 Sigma (nm)	2.14

EPE Histogram (Mask)



Mask Plane Metrology: What is the Target for EPE?

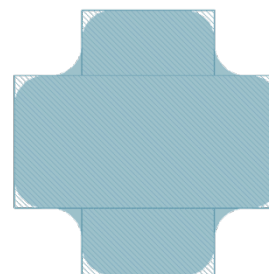


Mask Shape



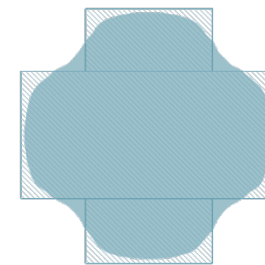
OPC Design

- No corner rounding
- Affected by corner EPE



CR + bias

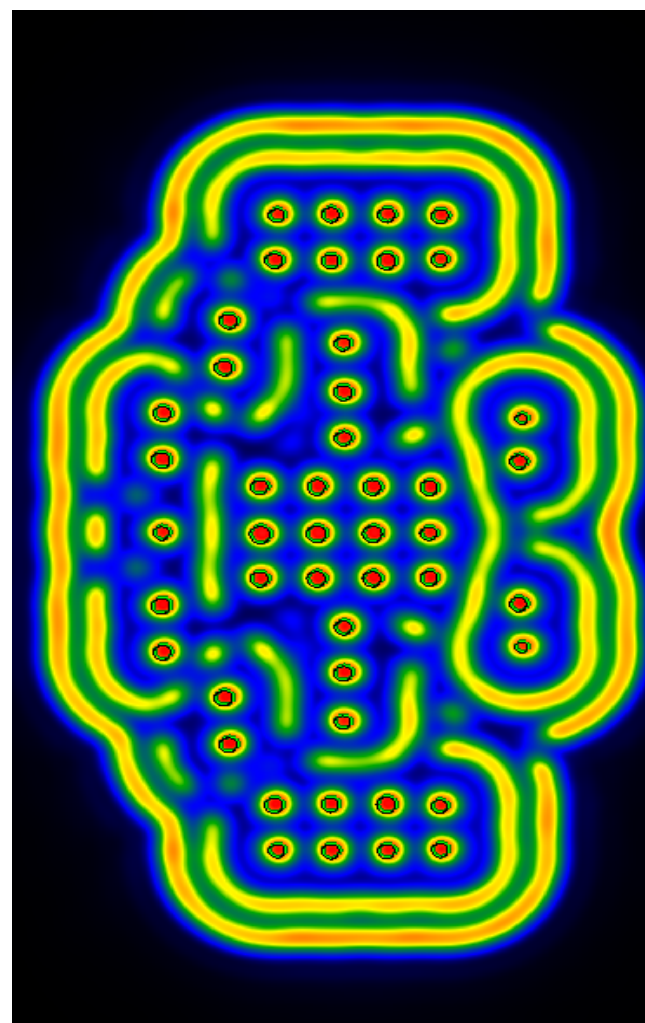
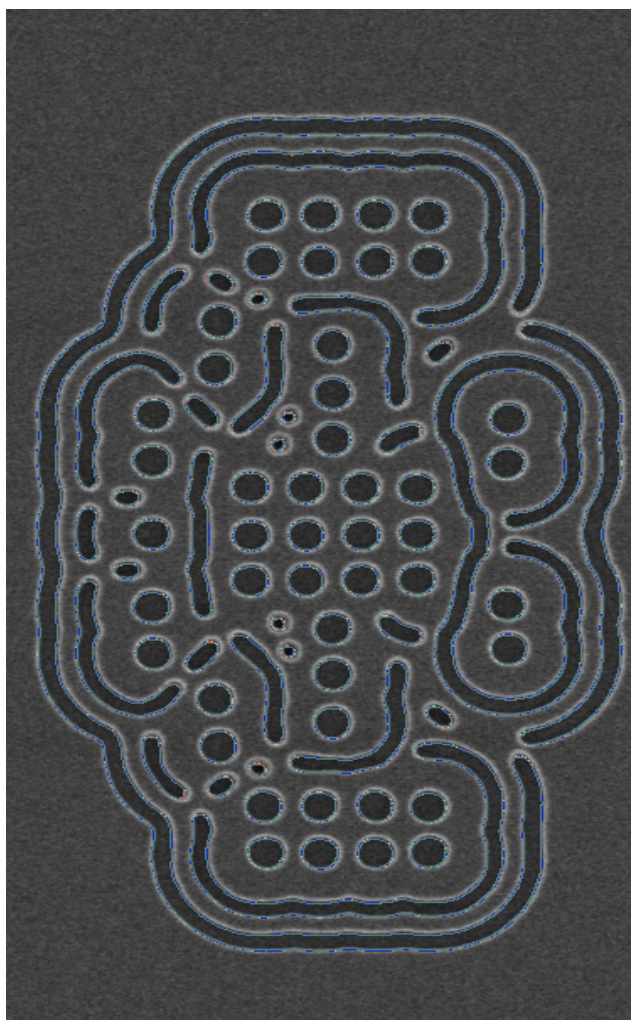
- What OPC thinks the mask shape will be



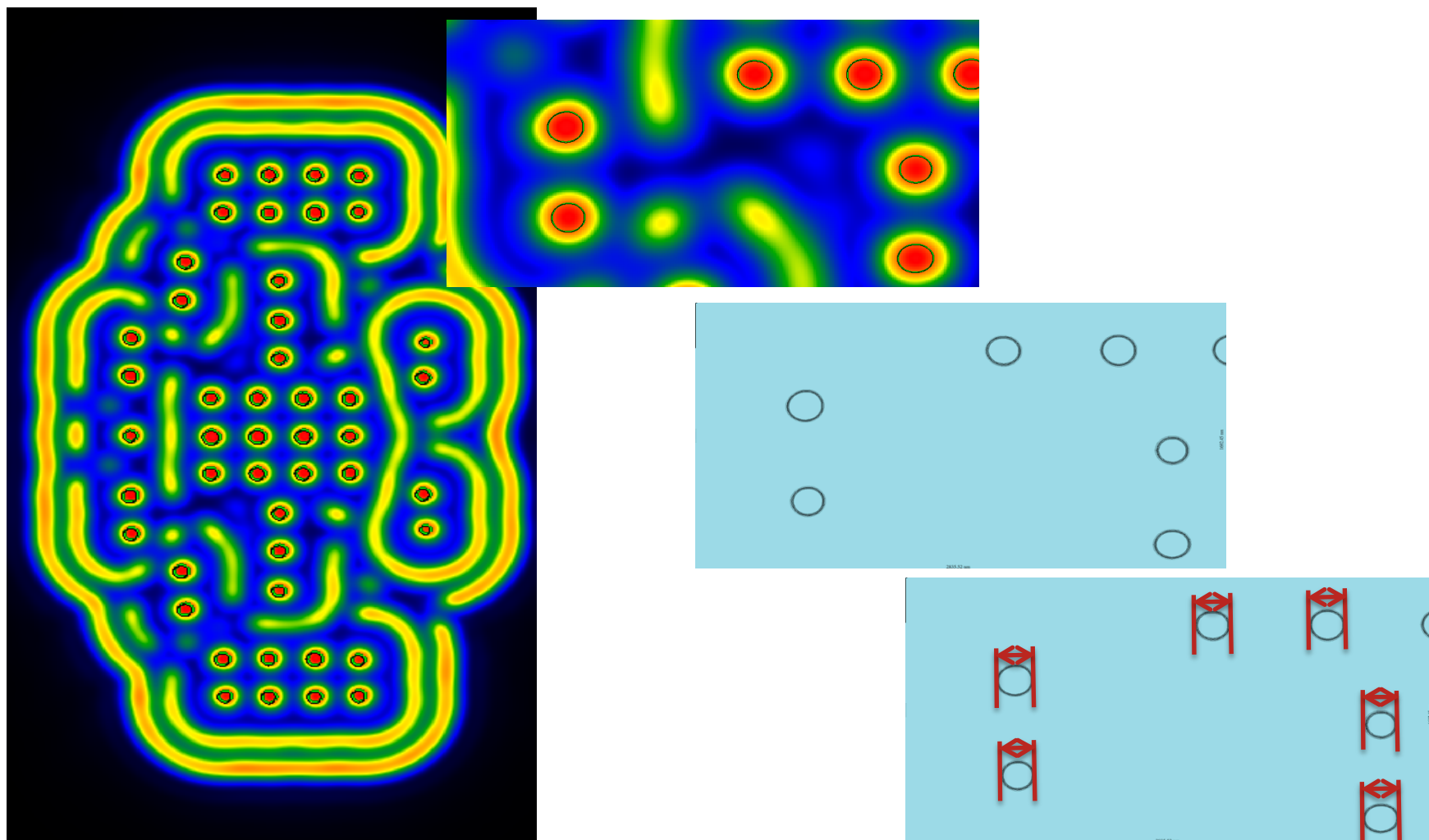
Simulated mask pattern

- Model of actual mask shape

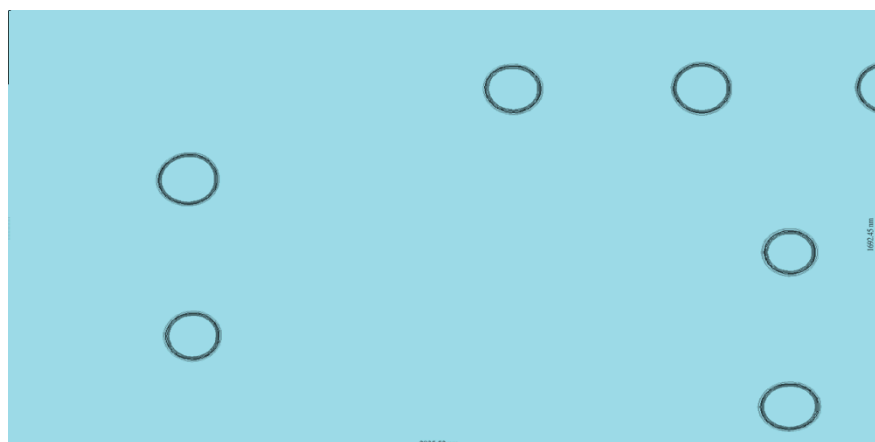
Wafer Plane Metrology: Traditional CD and Wafer Impact in One Simulation



Wafer Plane Metrology: Traditional CD and Wafer Impact in One Simulation

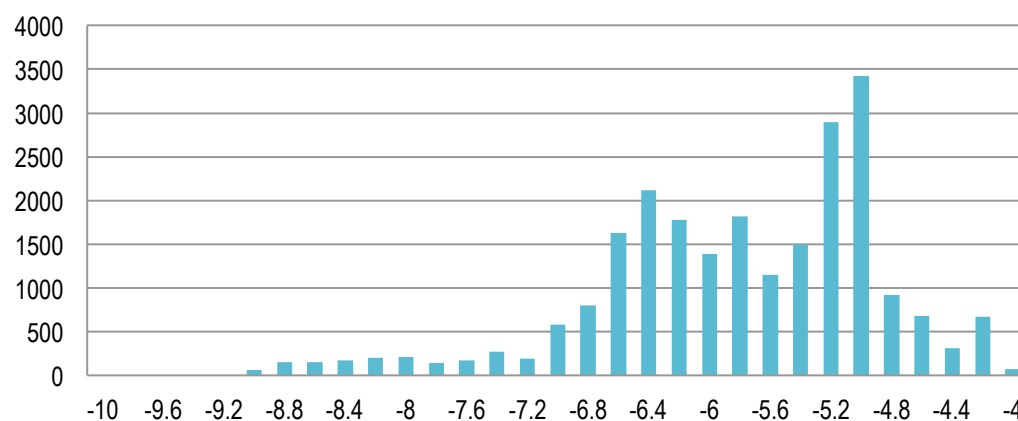


Wafer Plane Metrology: Traditional CD and Wafer Impact in One Simulation



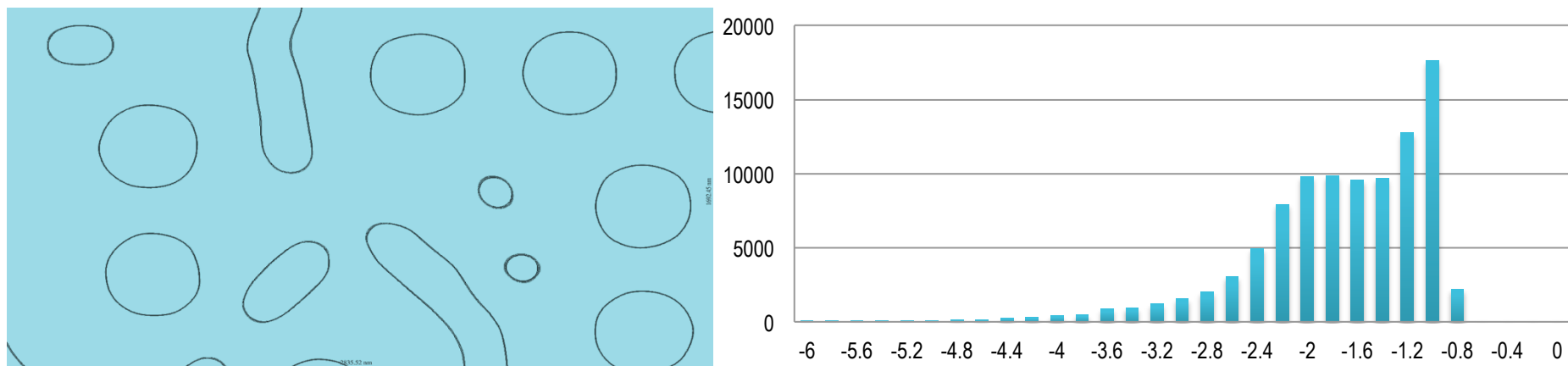
Count	23468
Min (nm)	-9.14
Max (nm)	-4.12
Mean (nm)	-5.91
Median (nm)	-5.81
3 Sigma (nm)	2.80

EPE Histogram (Wafer)

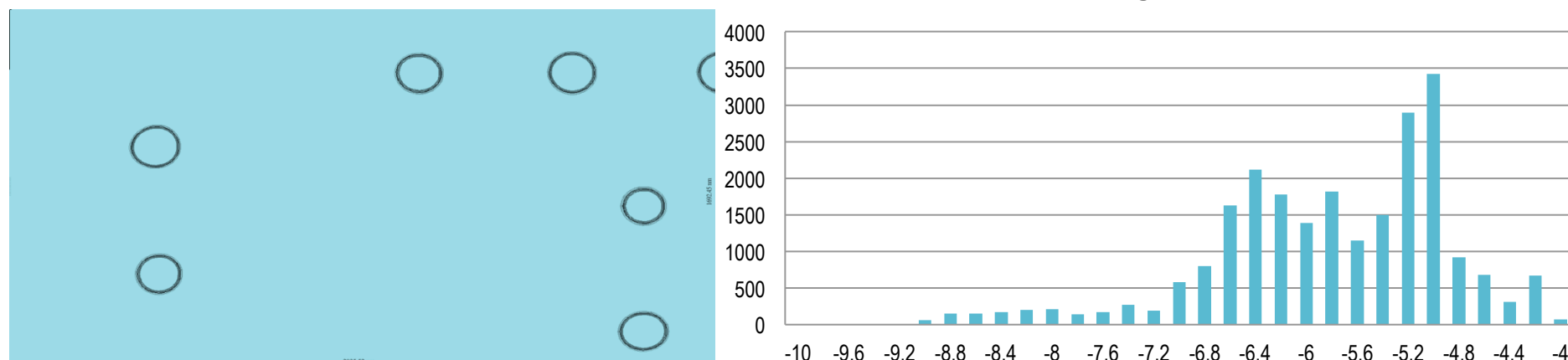


Mask CDU \neq Wafer CDU: Wafer Metrology is Required

EPE Histogram (Mask)

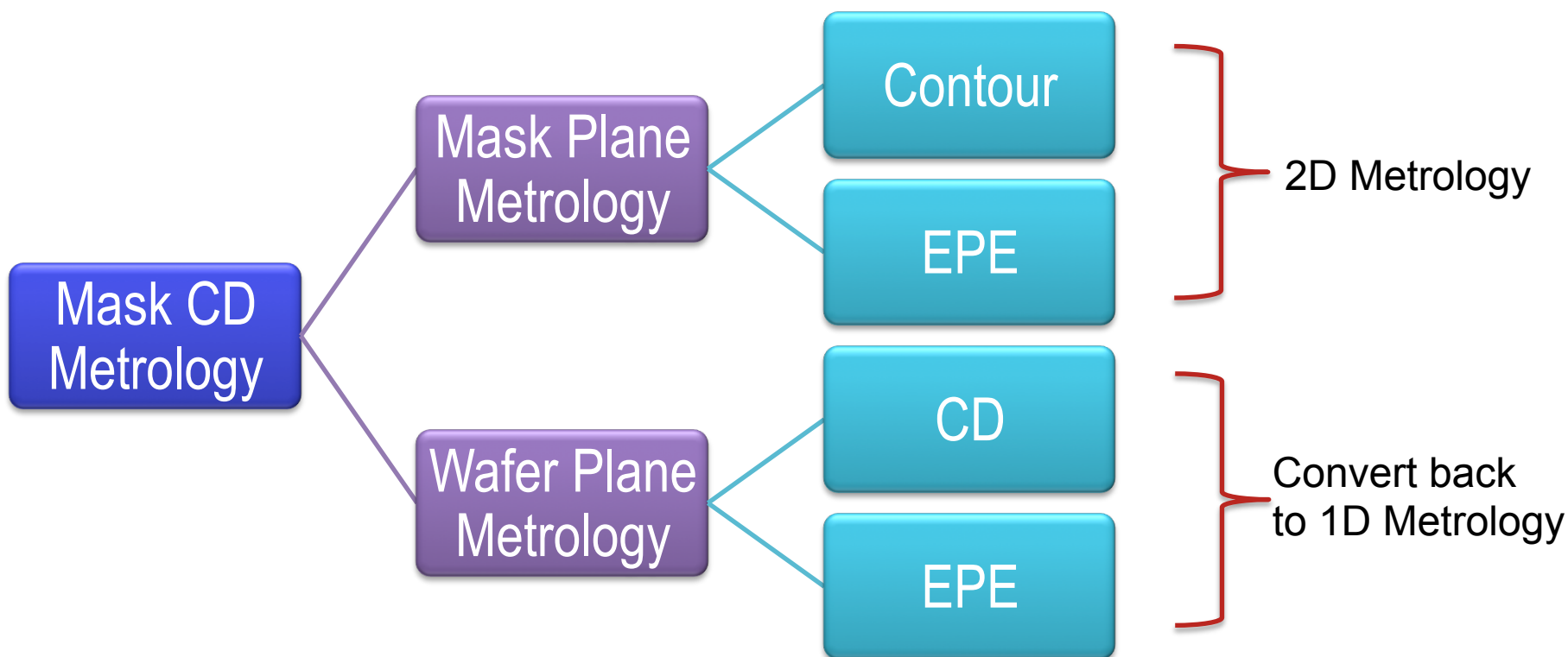


EPE Histogram (Wafer)

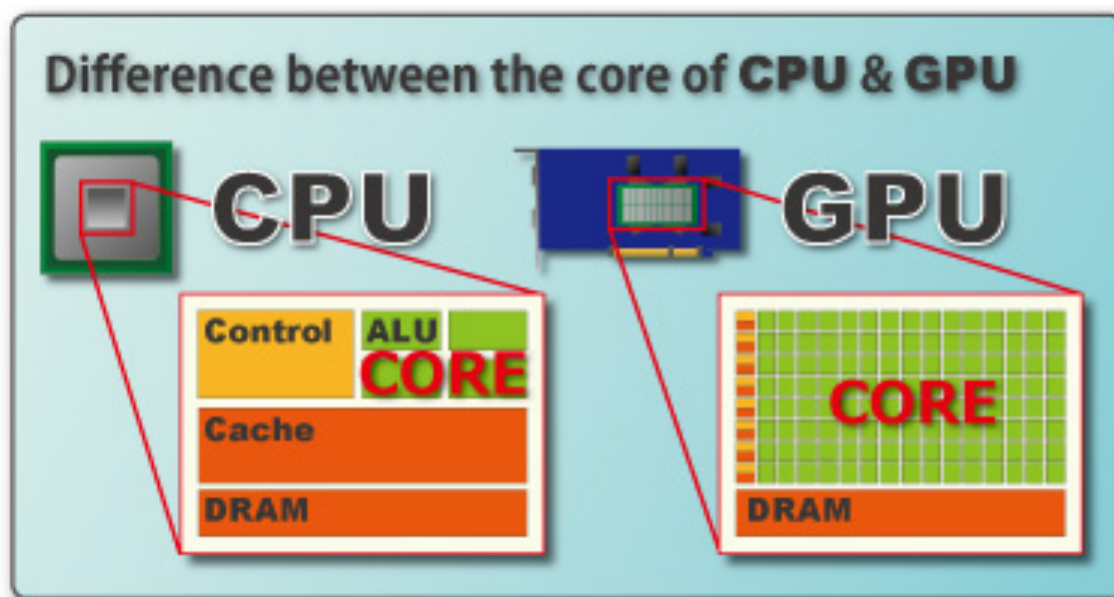


Old World: Mask CD Only

ILT World: Mask and Wafer

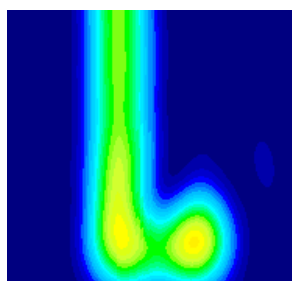
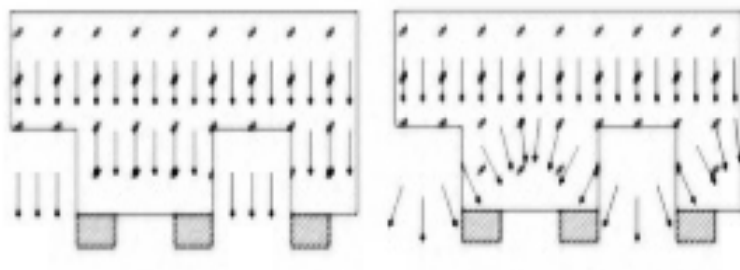


With GPU, the Simulation-based Wafer Plane Metrology is Real Time

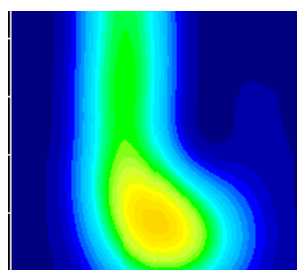


With GPU, the Simulation-based Wafer Plane Metrology is Real Time

Mask



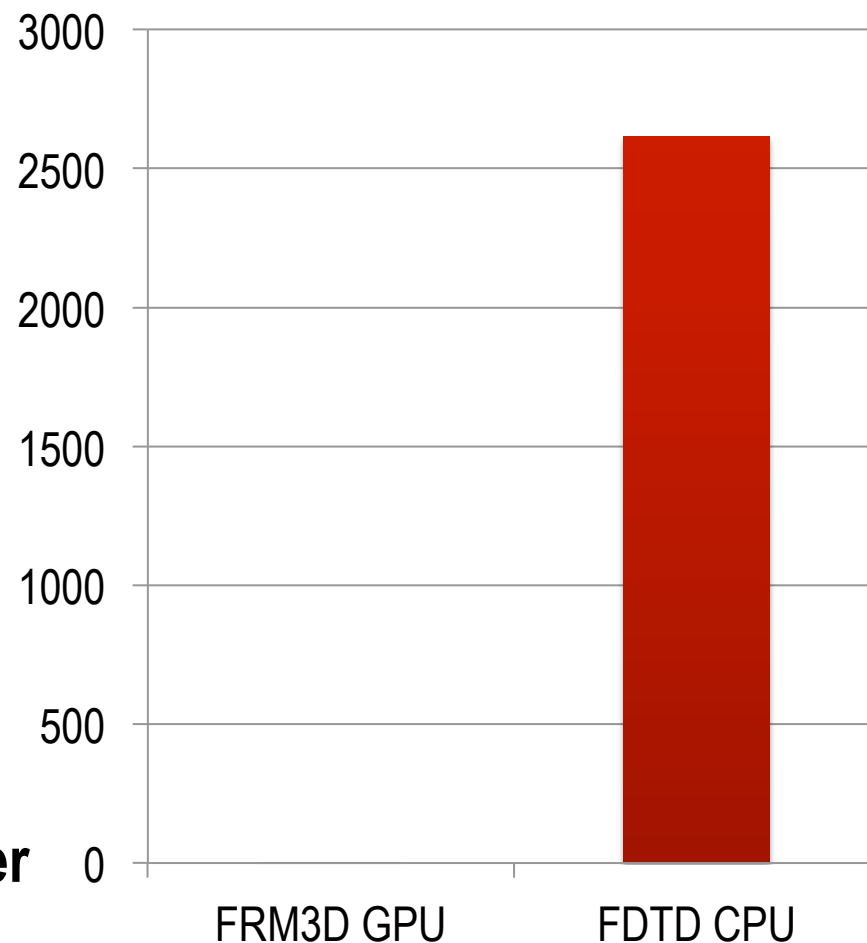
2D



3D

Aerial image

Runtime (seconds)

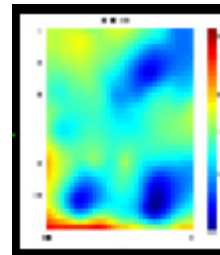


GPU 3D mask sim >1000 times faster

Future: Improve Mask and Wafer Quality



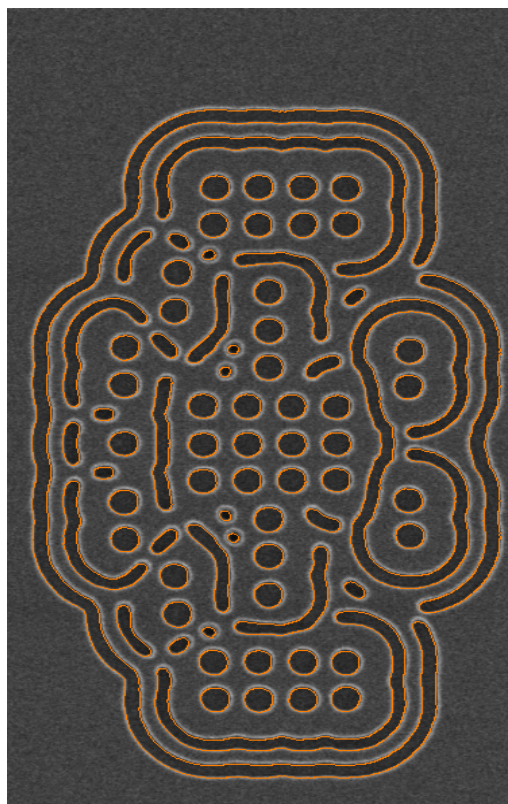
- Improve mask writing



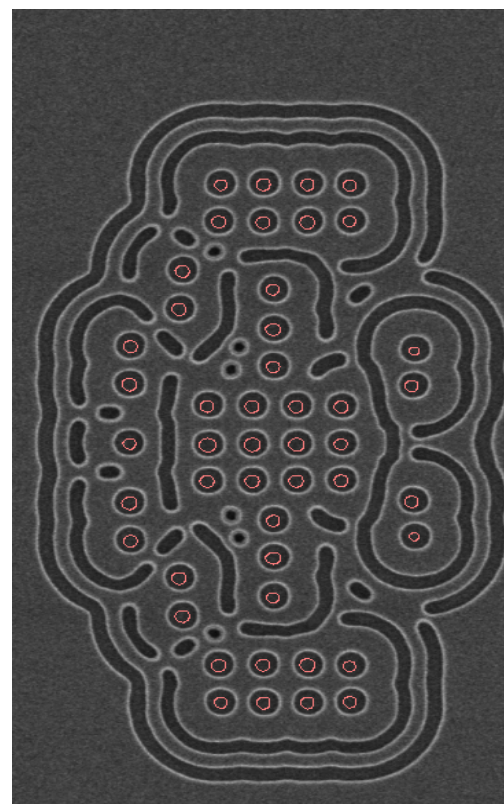
- Shorten time to get wafer CDU map
- Attain SEM-level repeatable accuracy

The New ILT World Calls for New CD Metrology: Mask and Wafer!

Mask

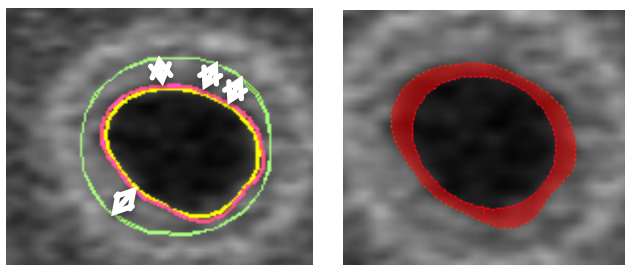


Wafer

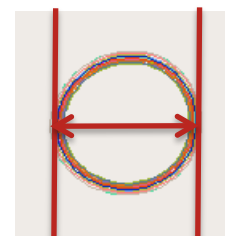


The New ILT World Calls for New CD Metrology: Mask and Wafer!

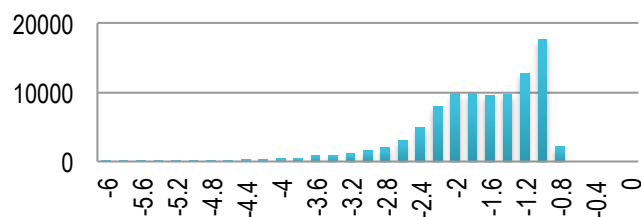
Mask



Wafer

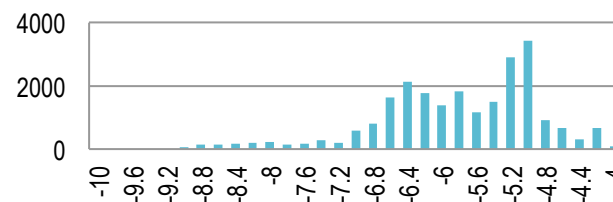


EPE Histogram (Mask)



Contour, EPE,
PV Band, Histogram

EPE Histogram (Wafer)



CD, EPE,
PV Band, Histogram

GPU = Real-time for mask + wafer

