



A Study of Wafer Plane Analysis with Mask MVM-SEM® using 2D and 3D Images

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1. Motivation Background

- DUV extension through 1Xnm technology node and beyond is a consensus in the industry
- The management of mask defects which are to be transferred onto wafer becomes much more important.
- The photomask pattern becomes smaller and more complicated due to RET technologies such as Inverse Lithography Technology(ILT) and Optical Proximity Correction (OPC) with Source Mask Optimization (SMO).
- Verification of mask defects with optical method is challenged due to its insufficient resolution in such advanced technology environment.





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1. Motivation Background

In this study

• We evaluated the correlation between our method using 2 dimensional (2D) images and aerial image microscope.

• In order to improve accuracy of defect printability analysis in the future, we applied 3 dimensional (3D) information of CDs and studied if we can improve simulation accuracy for future nodes.





2. Mask Defect Review and Printability Analysis Flow (1)



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2. Mask Defect Review and Printability Analysis Flow (2)



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3. Influence of FOV size to simulation accuracy



CD on wafer: 56.0nm CD on wafer: 57.9nm AIMS[™] result: 56.0nm (1/4 mask scale)

CD difference is 1.9nm on wafer plane in case of small field.

Large field image with Mask MVM-SEM[®] enables accurate lithography simulation.



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4. Large FOV 2D Simulation Correlation



	Reference(nm)	Defect(nm)	Diff. (%)
MVM SEM+LithoSim	307.018	263.248	-14.3
AIMS™	307.004	261.935	-14.7
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5. Application of MVM-SEM® 3D Capability

- Mask MVM-SEM[®] detects top/bottom contour of mask surface as 3D information.
- By using such information, the system can characterize mask processes and verify mask quality more accurately.
- By monitoring mask manufacturing based on the characterization, the system can prevent and/or predict mask process excursion and pattern failure.



6. 3D Lithography Simulation Study (1)



They show significant difference; Sidewall angle needs to be measured and considered in simulation.



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6. 3D Lithography Simulation Study (2)

Extracted 3D SEM mask contour EUV half pitch 80nm L/S on mask \Rightarrow 20nm expected on wafer.



SEM Contour of Bottom layer

Extracted mask contour by 3D measurement capability will be useful for more accurate lithography simulation with 3D mask model.



7. Conclusions

- Large field image captured with Mask MVM-SEM[®] enables accurate lithography simulation.
- Correlation between our simulation methodology and AIMS[™] tool using 2D SEM images has been confirmed.
- Such methodology can reduce AIMS work load, therefore can reduce turn around time of mask manufacturing.
- In addition to 2D cases we studied 3D simulation for masks in advanced technology nodes.
- It is found that sidewall slope has a large effect on simulated CDs (>10%). Hence, the real sidewall slope profile must be used.



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7. Conclusions

We believe that this CD verification system with Mask MVM-SEM[®] and mask/wafer double lithography simulation technology can contribute to improvement of mask processes for advanced technology nodes.

 D_{2S}

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