5NM TEST CHIP DESIGN & MANUFACTURING CHALLENGES: AN EUV VS 193i COMPARISON

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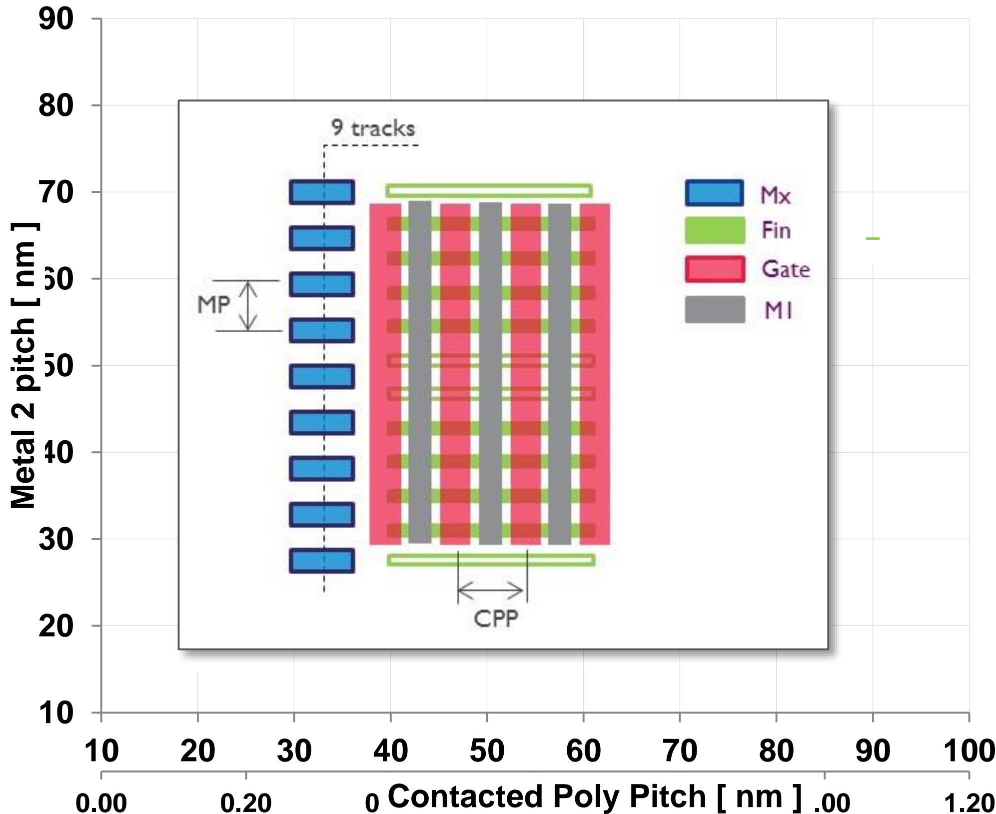
Presented at the eBeam Initiative SPIE lunch
February 2016

LOGIC SCALING LANDSCAPE



- MP x CPP x track height determines logic cell area
  - Gate pitch (CGP or CPP)
    - Determines x-dimension
    - #CGP determined by cell complexity
  - Mx pitch (MP) together with track height
    - Determines y-dimension
    - Track height is constant for logic library and determines area available for active and routing

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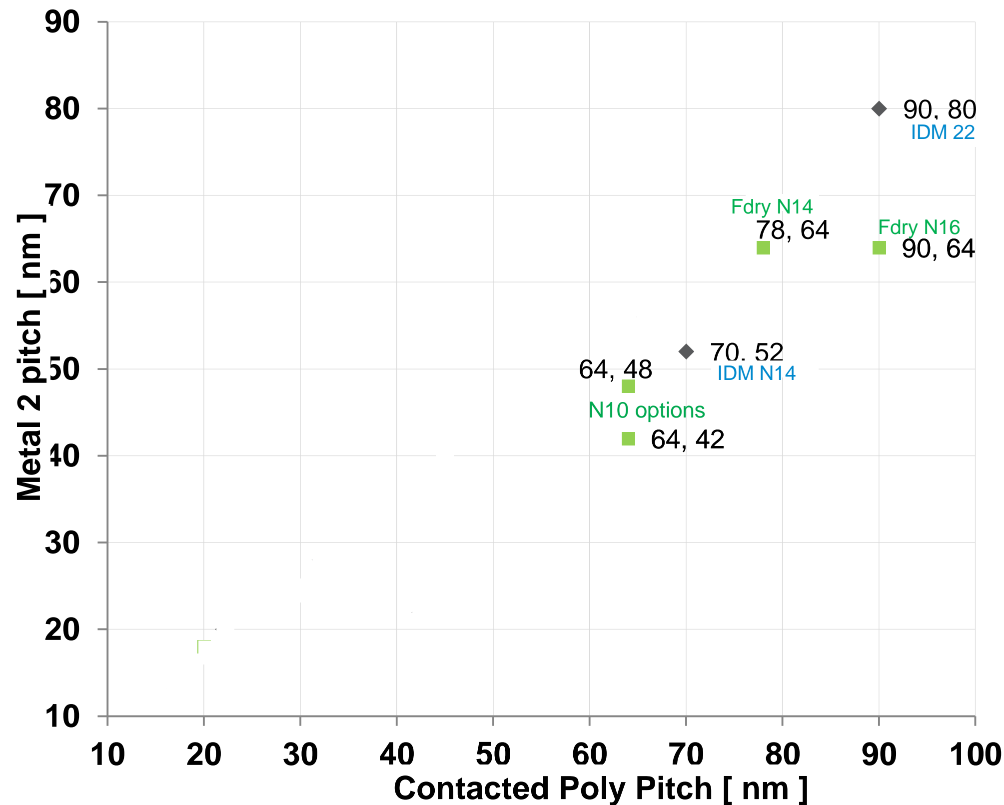
LOGIC SCALING LANDSCAPE

Nodes today in the market



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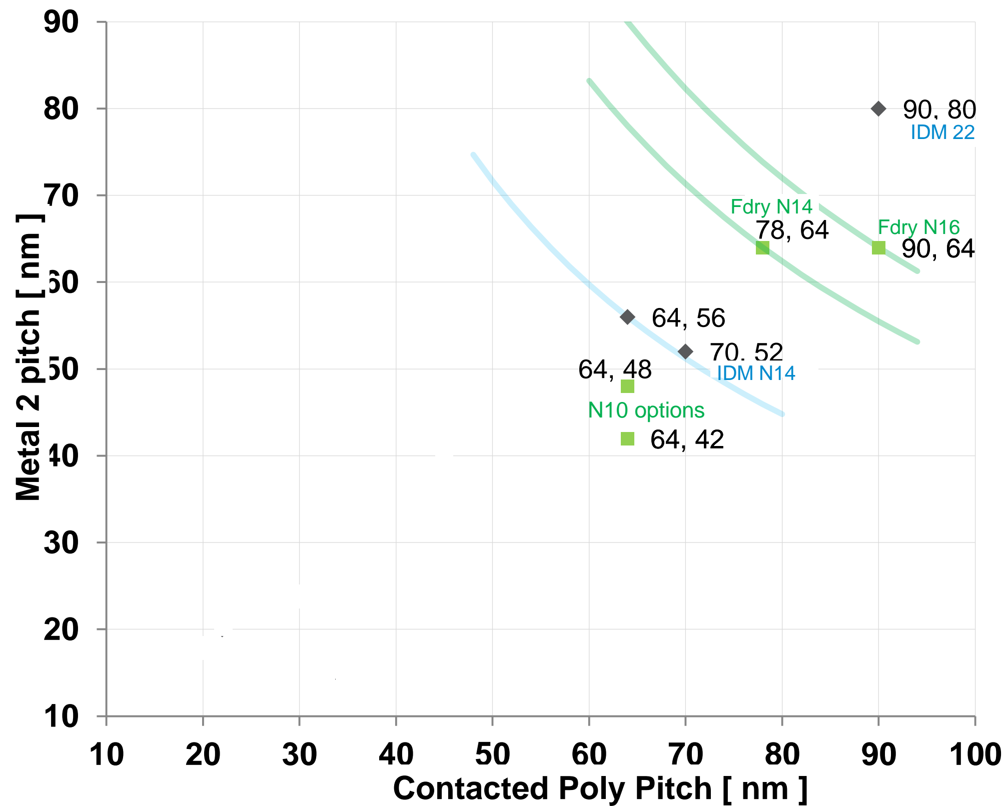

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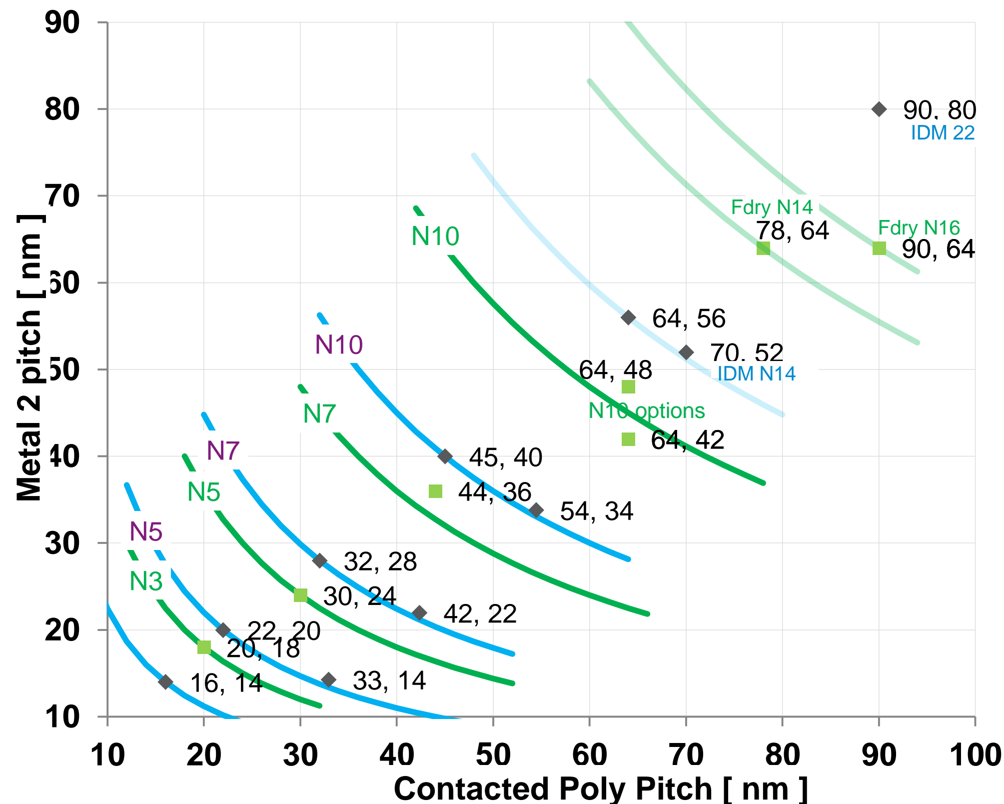
LOGIC SCALING LANDSCAPE

Scaling options down to N7 and N5



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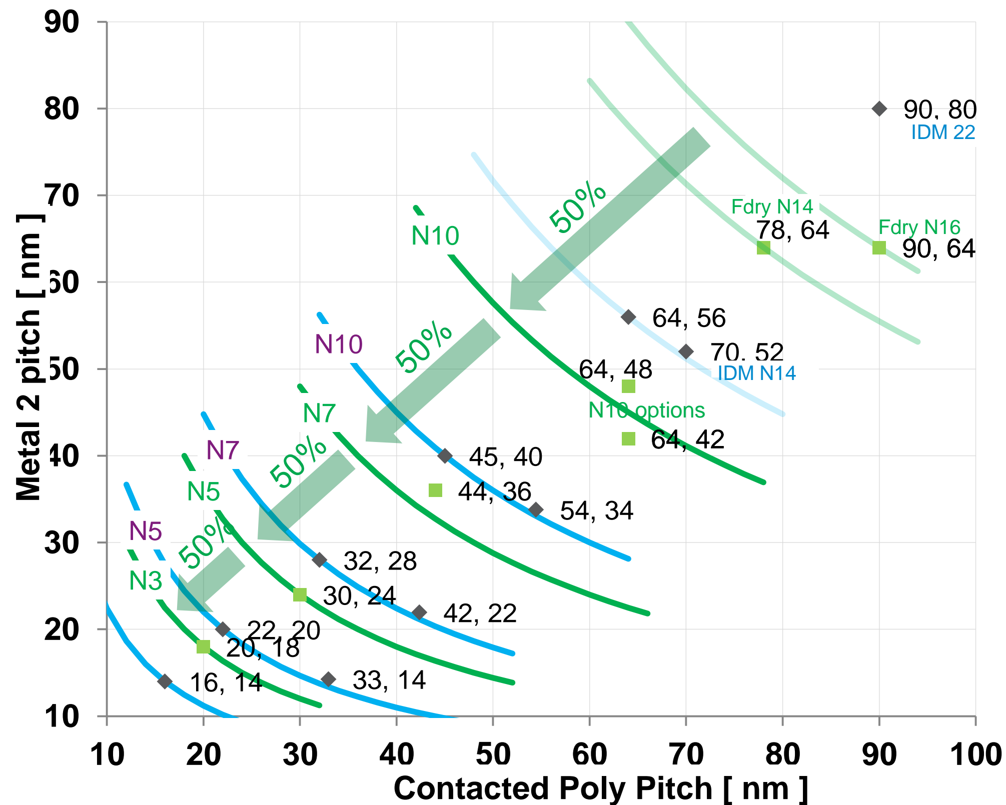
LOGIC SCALING LANDSCAPE

Scaling options down to N7 and N5



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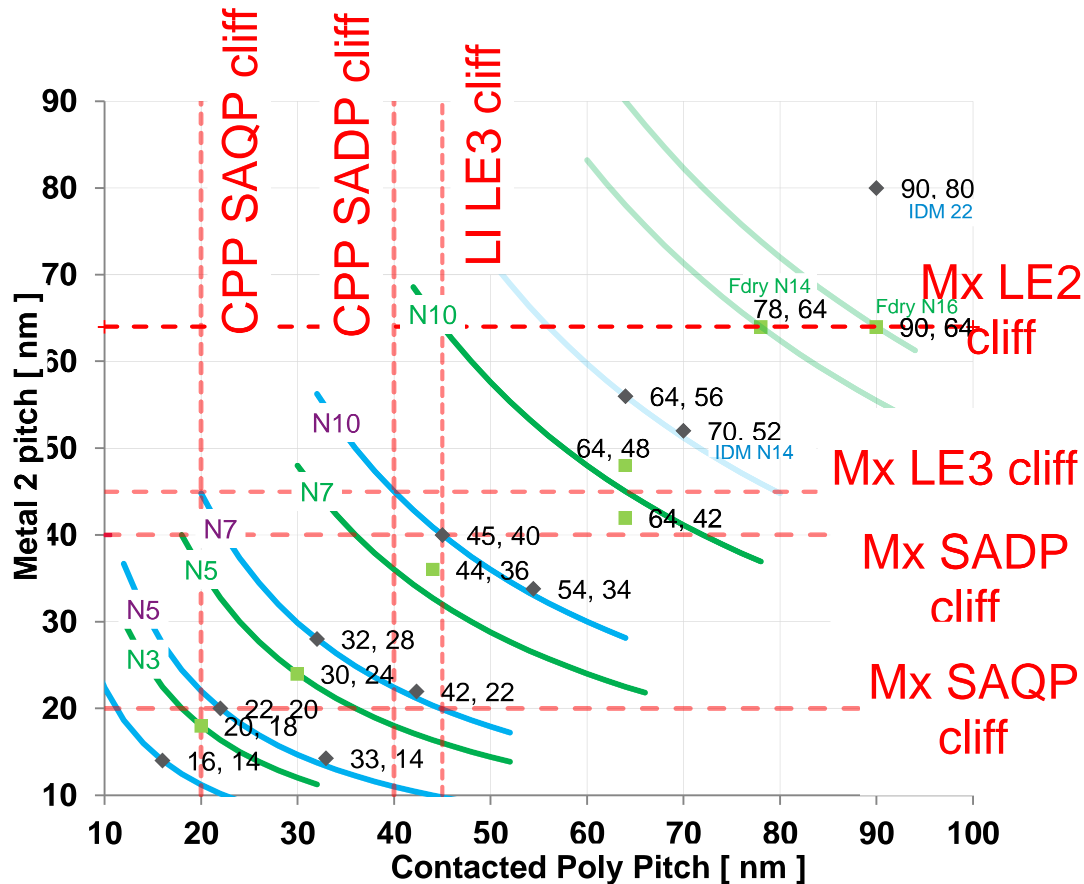
LOGIC SCALING LANDSCAPE

Patterning cliffs determine cost vs area trade-offs!



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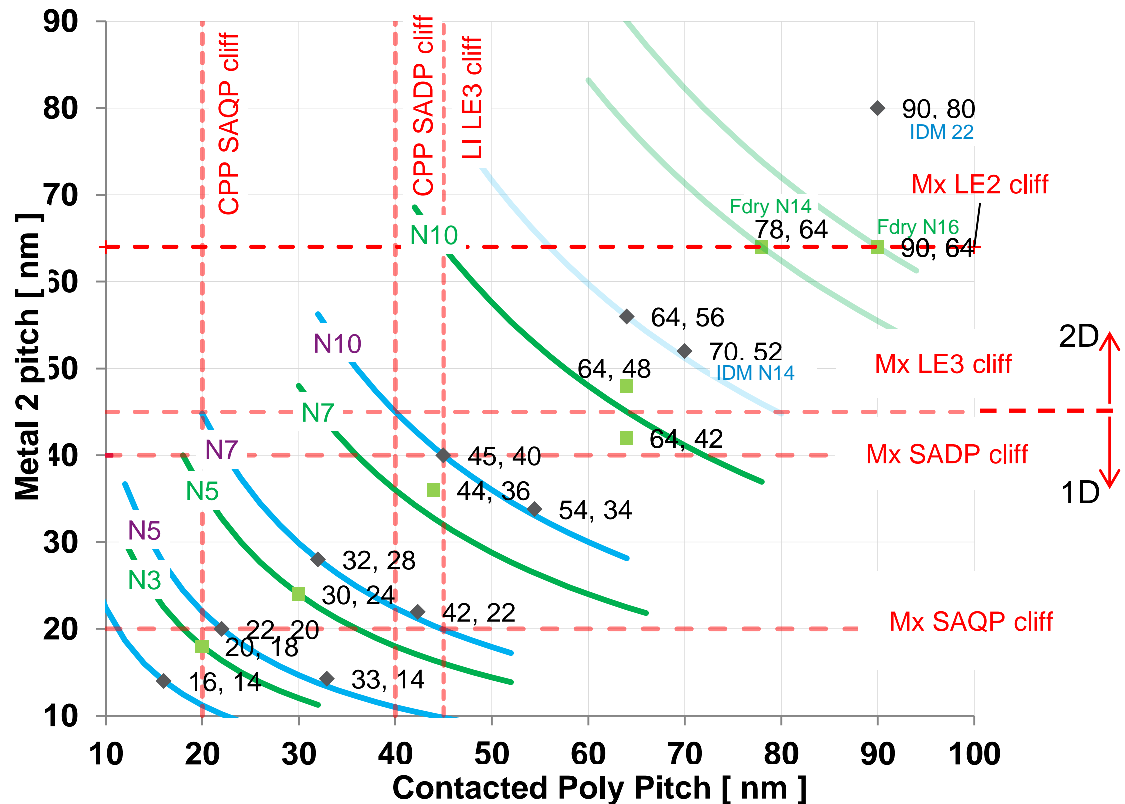
LOGIC SCALING LANDSCAPE



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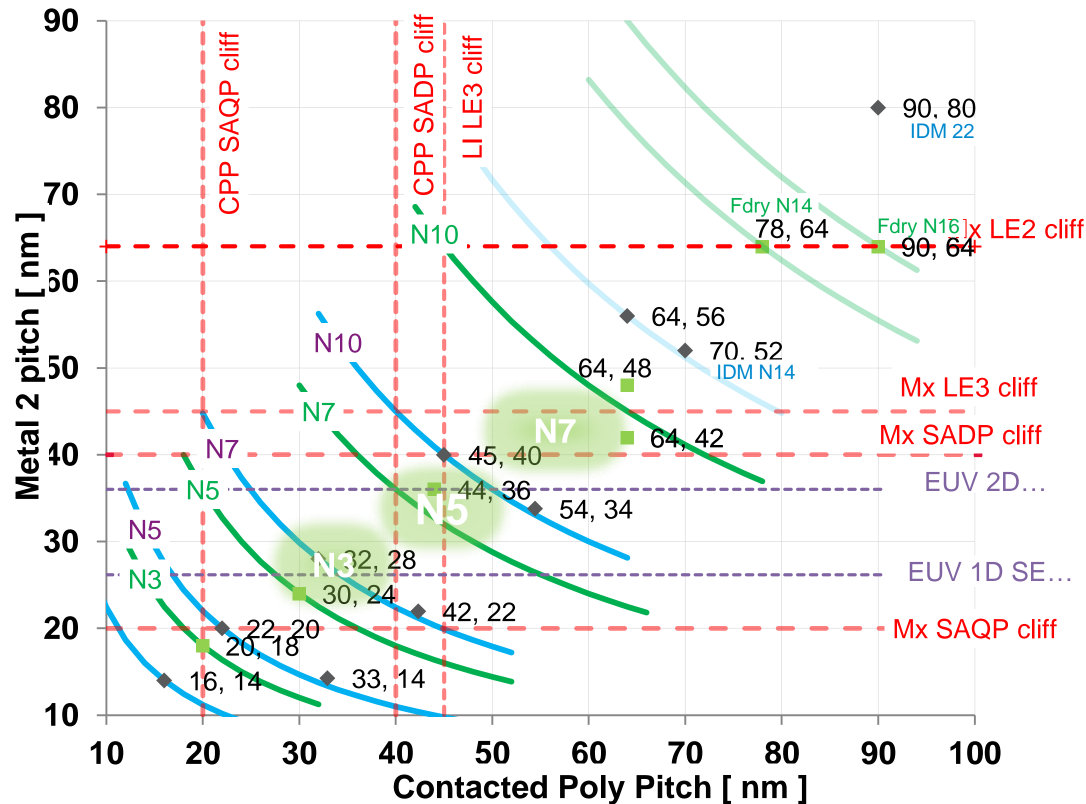
LOGIC SCALING LANDSCAPE

Pragmatic node naming conventions



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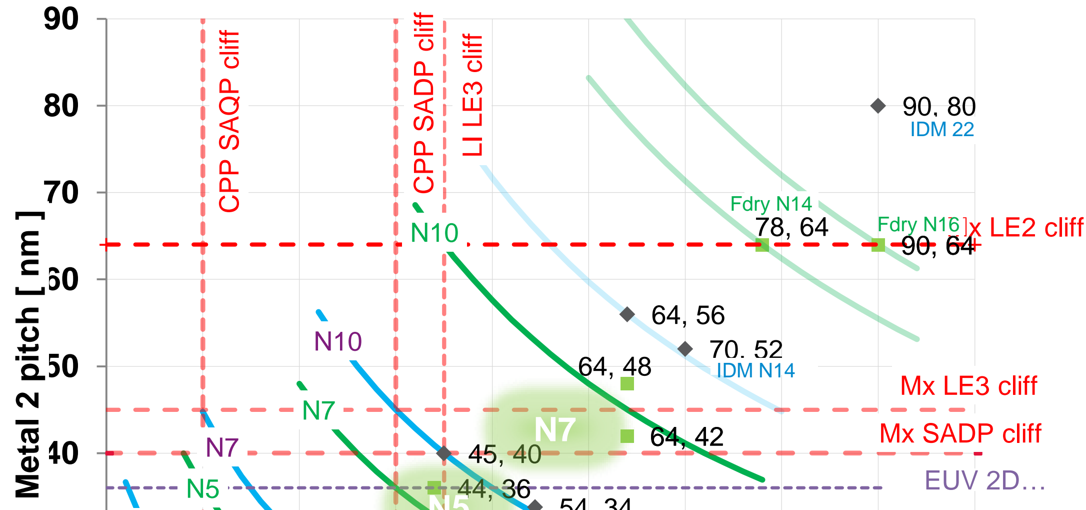
LOGIC SCALING LANDSCAPE

N7/N5: Many options open up for patterning

Making the problem challenging and interesting!



- Pitch range from 34nm down to 24nm have many options for patterning
- EUV 2D
- EUV 1D
- SAQP
  - Different block schemes
- LE3

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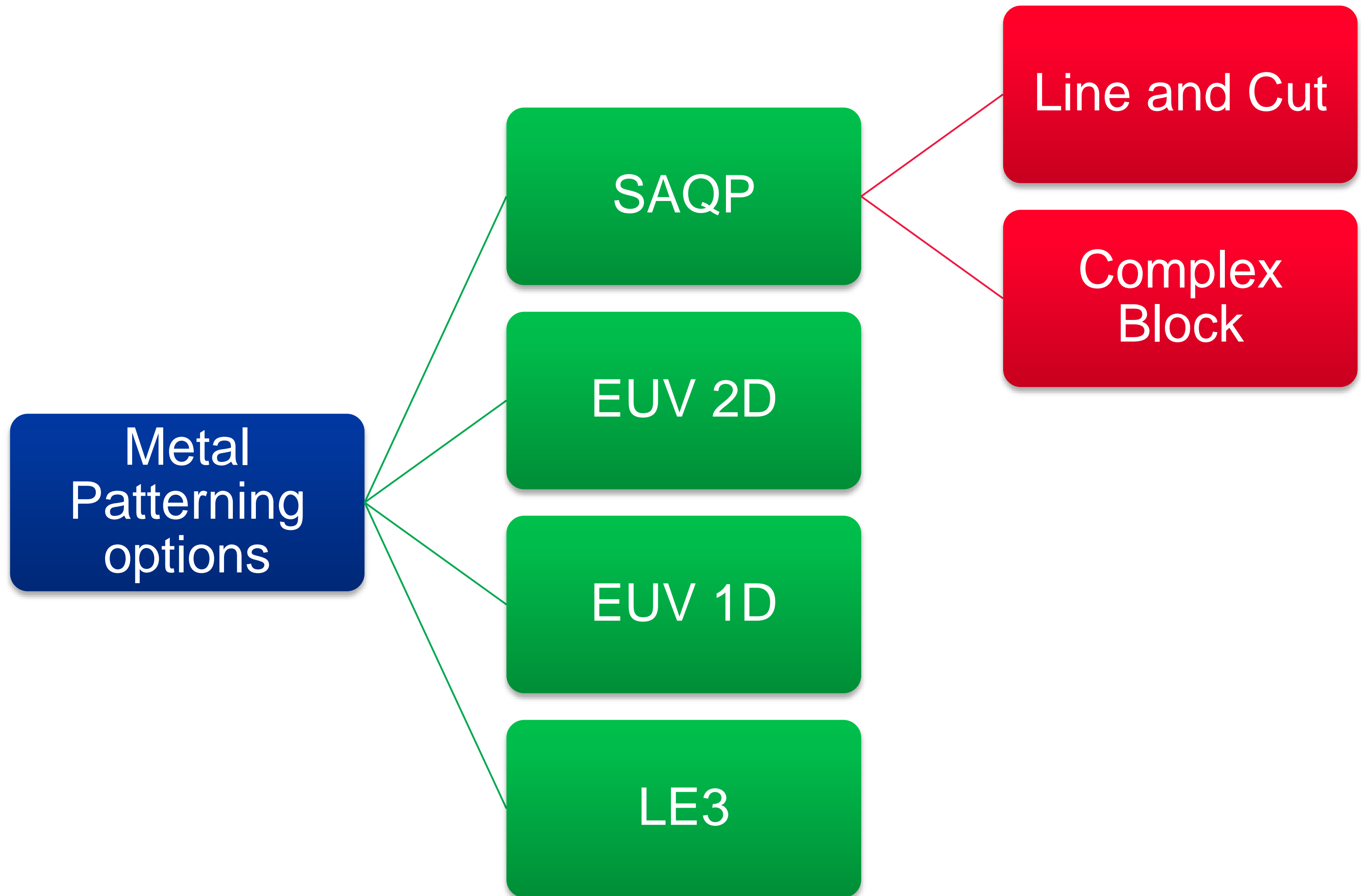
EARLY TEST CHIP NEEDED
TO UNDERSTAND DESIGN RULE ARCS

OBJECTIVE OF TEST CHIP(S)

Evaluation of the various options



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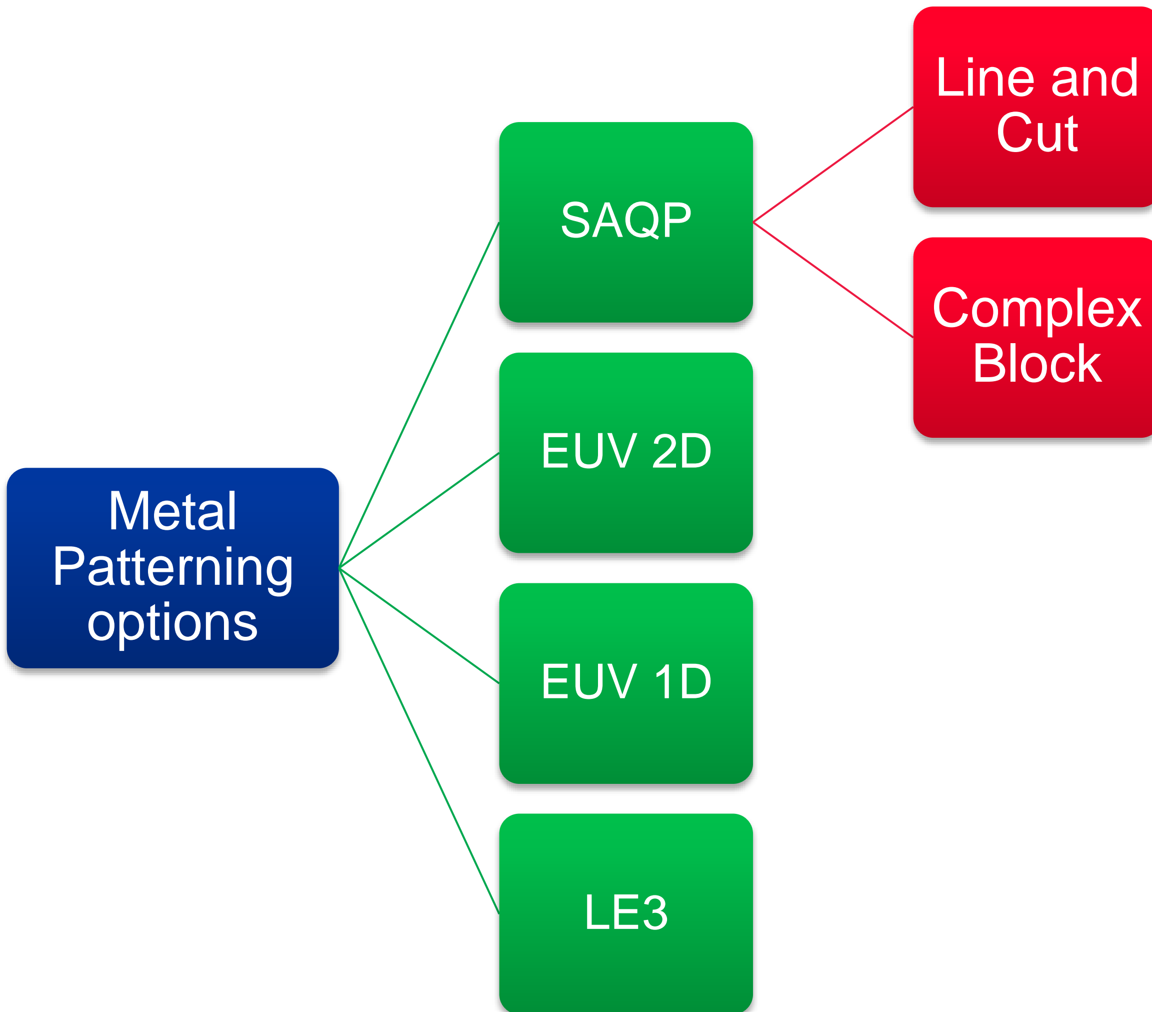
OBJECTIVE OF TEST CHIPS



- Understand the pitch limitation of each of these options
- Understand process window for each of these options
- Understand power-performance-area impact of each
- Under ‘product’ like context

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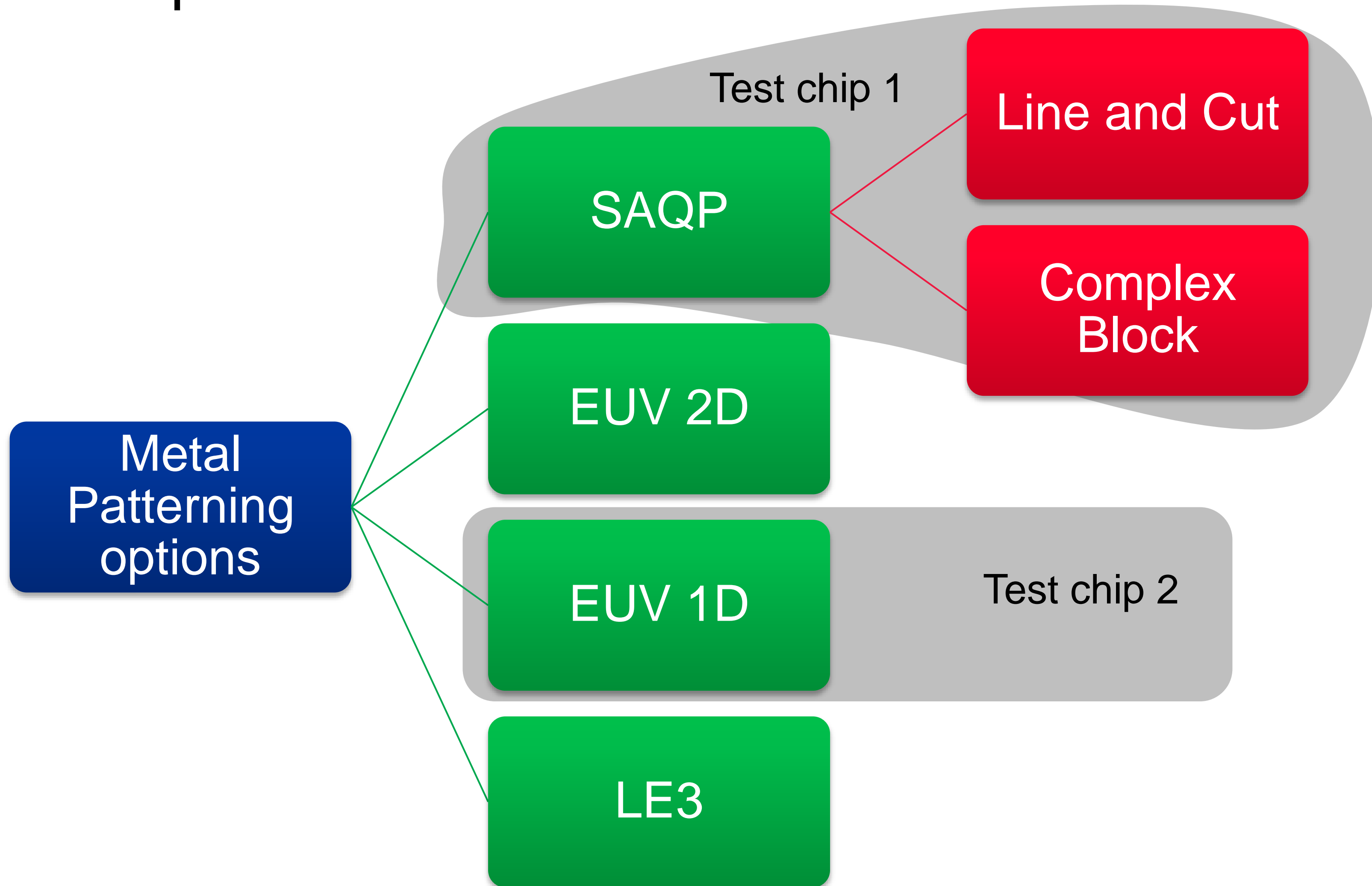
OBJECTIVE OF TEST CHIP

The various options



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WHAT'S ON THE MASKS

M1-via-M2 and M2-via-M3 taped out

Place and routed blocks of two digital IP blocks and SRAM content

Designs however were complete with all layers and appropriate digital design flows in place

- But only the M1-M2 and M2-M3 layers taped out

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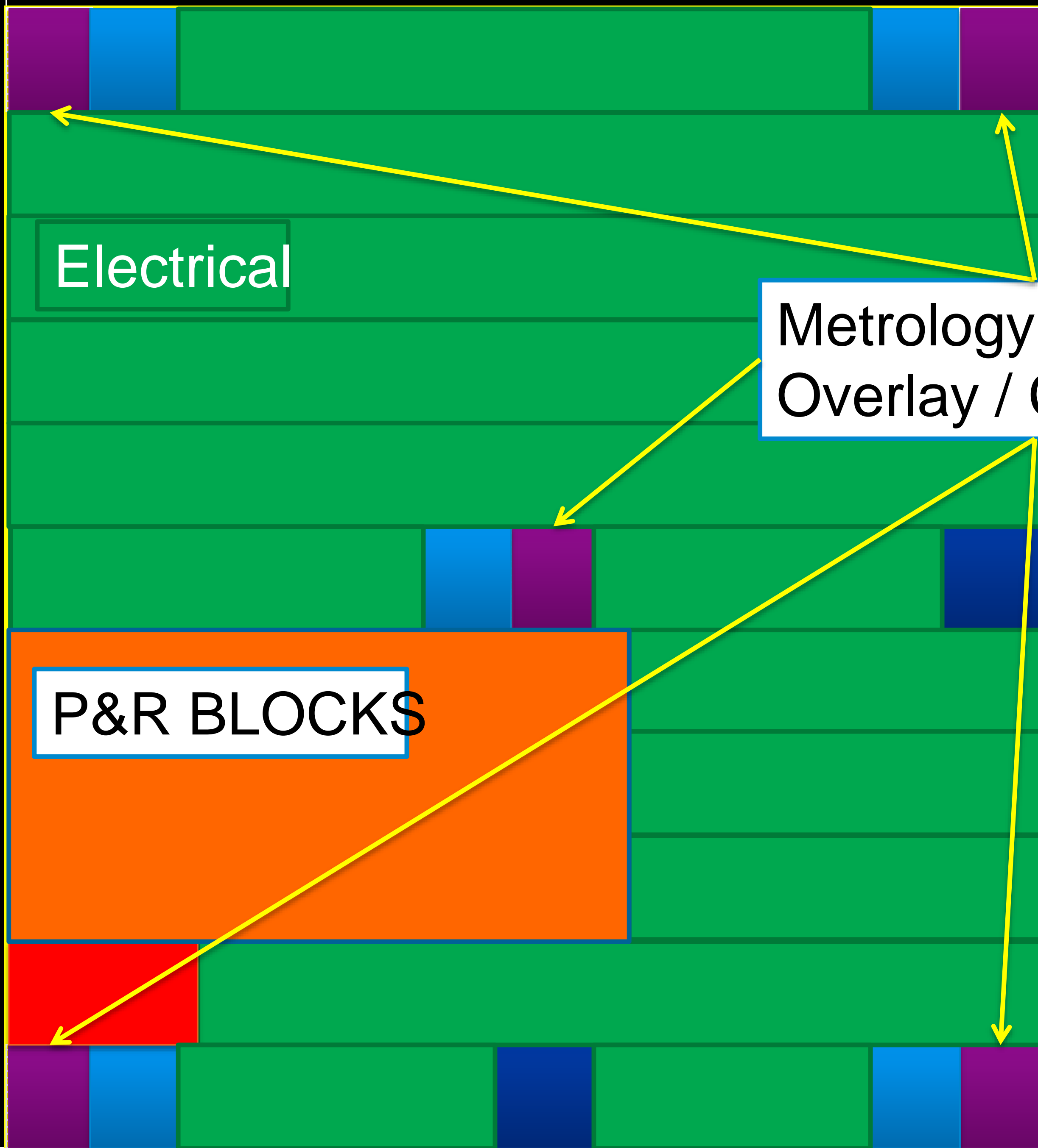
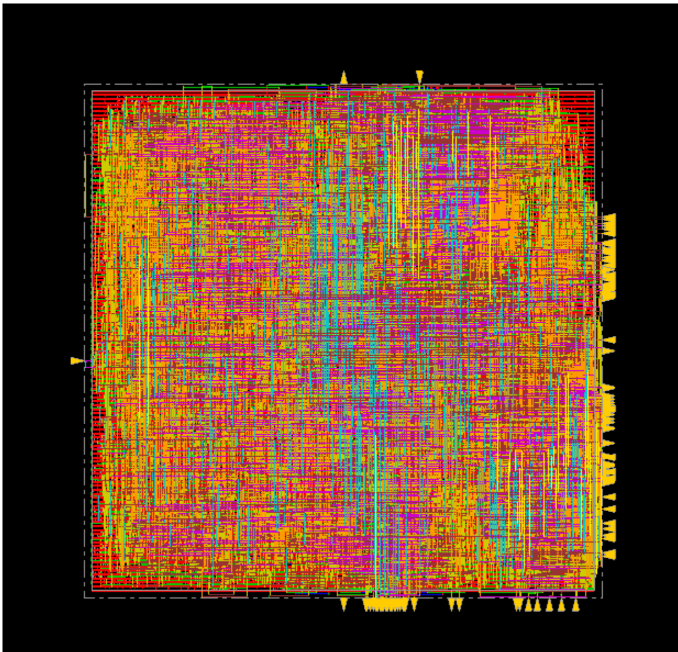

Electrical
Metrology Blocks
Overlay / CD control
P&R BLOCKS

Design Place and Routed in collaboration with

cādence™

IMEC designed 32-bit DSP Core

ARM® Cortex®-M0



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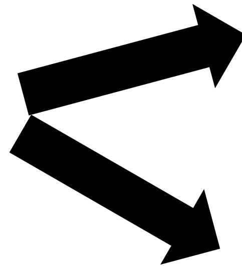
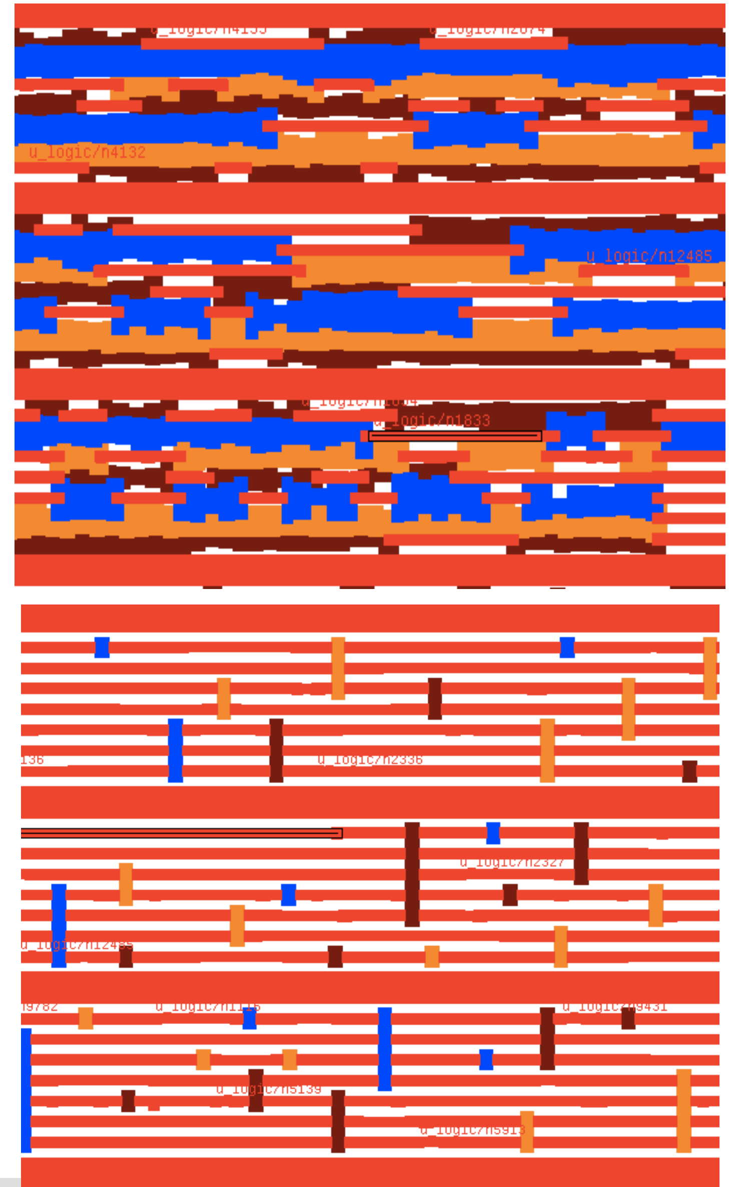
TEST CHIP 1: SAQP PATTERNING

Intent of designer



Option 1:
Remove all dummies

Option 2:
Make simple
lines and cuts



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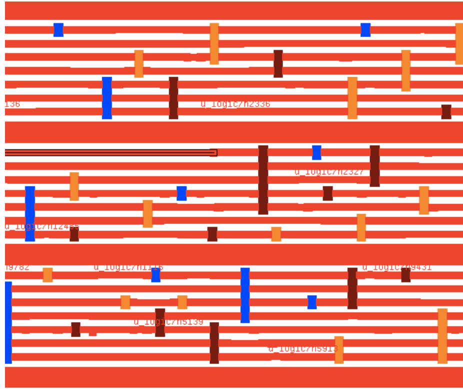
TEST CHIP 1: SAQP COMPARISON

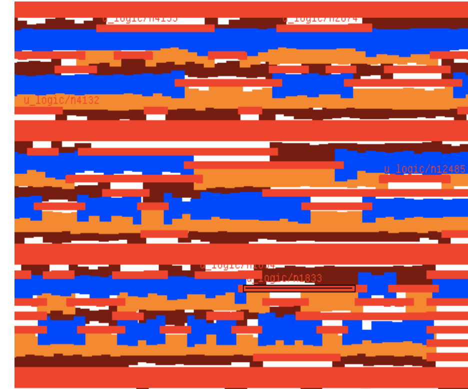


Good CDU and variability control due to SAQP metal

Simple cut mask strategy

Multi color cut mask needed to maintain design completion

- 32nm MP → 3 cut masks in 193i → 1 cut mask in EUV
- 24nm MP → 4-5 cut masks in 193i → 1 cut mask in EUV



Good CDU and variability control due to SAQP metal

Complex masking strategy to remove all dummies and stitching of masks

Multi color cut mask needed to maintain design completion

- 32nm MP → 3-4 cut masks in 193i → Likely no EUV solution as complex 2D shape at sub 32nm pitch!

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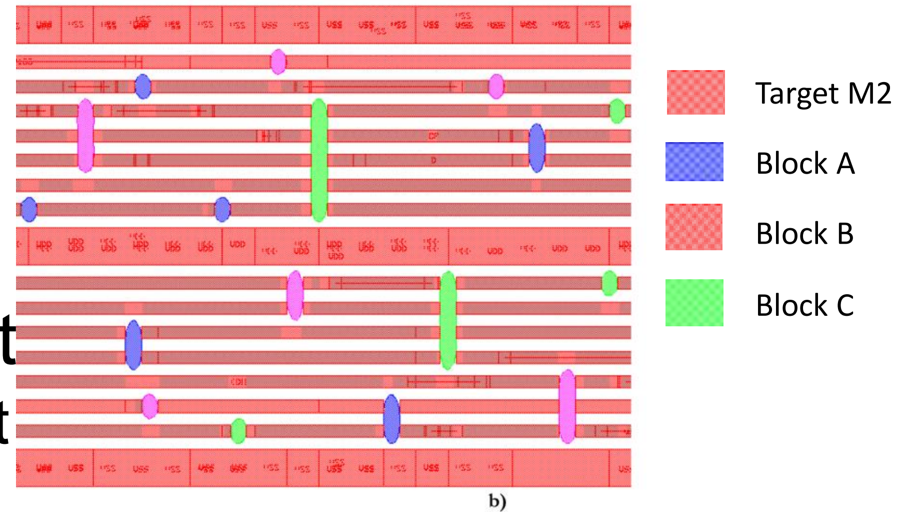
WHAT DO WE WANT TO LEARN?

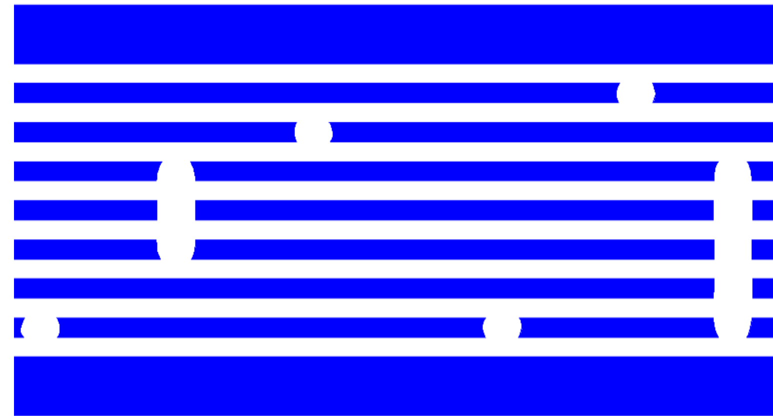
Its not just about lines and spaces!

Many secondary rules have a huge design impact

- What should be the cut to cut distance?
- What should be the via enclosure?
- What would be the EPE on cut?



b)



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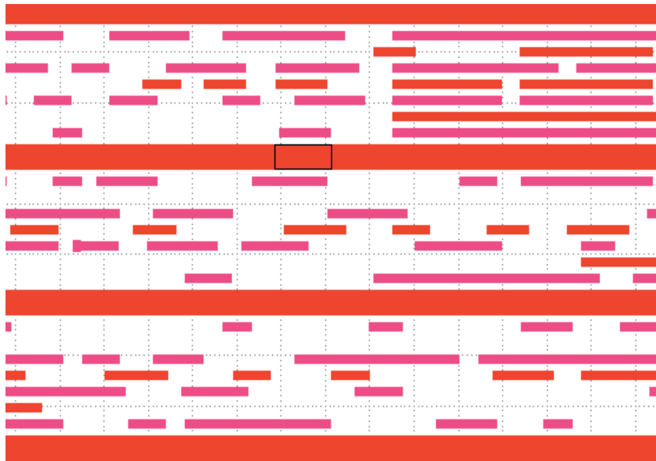
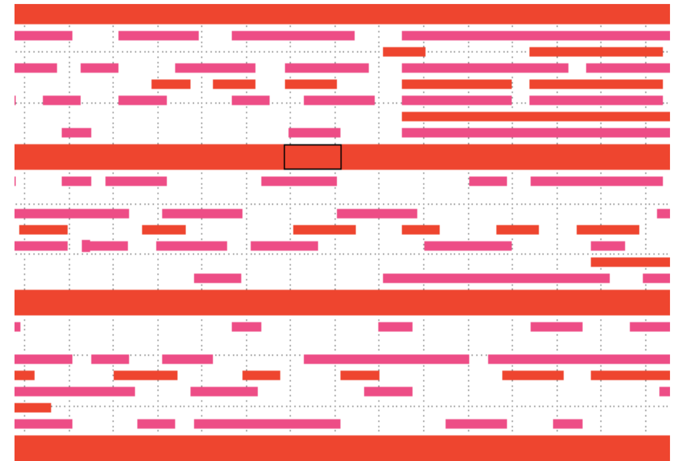
TEST CHIP 2: EUV PATTERNING

Intent of designer

Directly print the target intent using EUV





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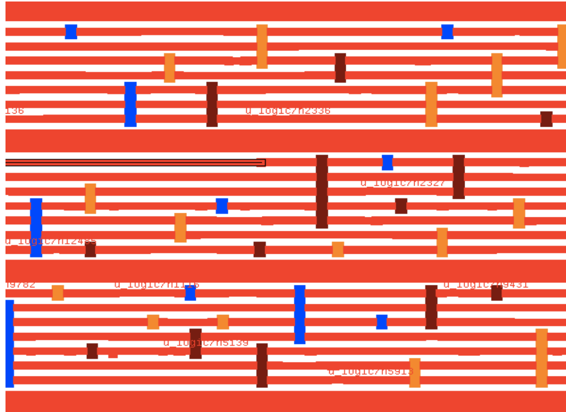
EUV VS SAQP COMPARISON



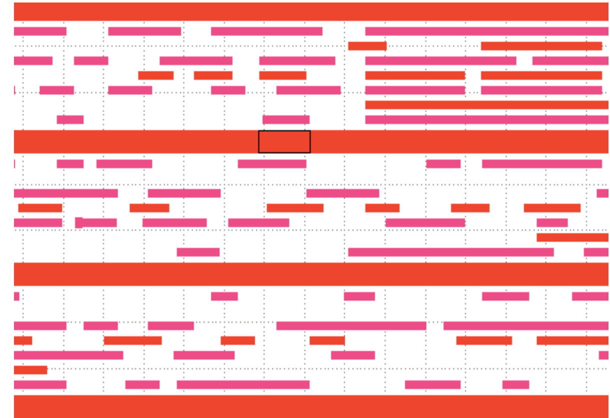
Good CDU and variability control due to SAQP metal

Scalability of SAQP to 20nm-24nm

Simple cut mask strategy

Lots of dummies

- Good for CMP: very good metal uniformity
- Increased capacitance due to coupling of dummy nets to active nets



CDU may be poorer due to EUV LER

1D EUV likely to scale down to 24-26nm

Some line pull back expected on lines

No dummies

- No increased capacitance!

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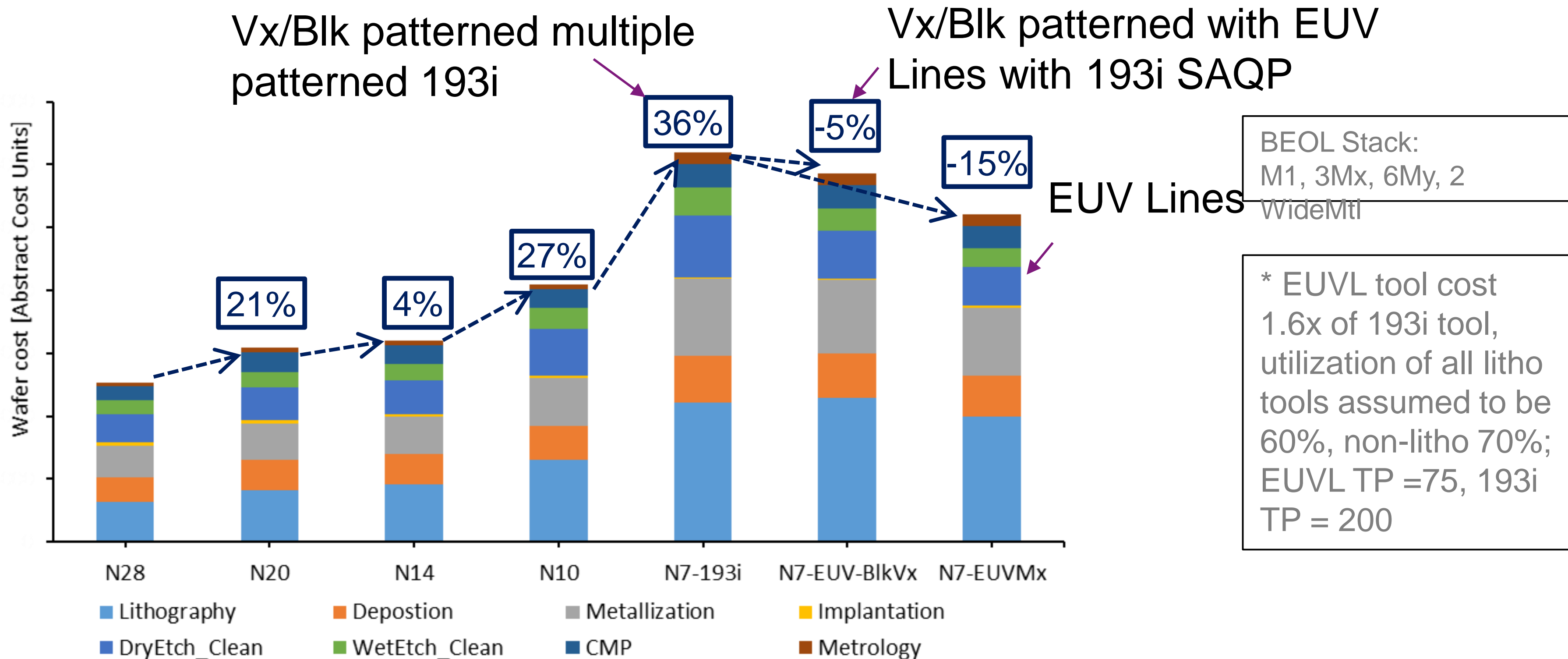
WAFER COST EVOLUTION
EUV VS 193i SOLUTION



- N7-EUVBLK option replaces the multi-patterned (LE^3 or more) block and via by EUV-SE to save 5% of the wafer cost
- Mx with EUVL results in significant wafer cost benefit and enables 2D BEOL

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CONCLUSIONS

We need to prepare for EUV and 193i solution space

Cost/power/performance of each solution may enable or postpone the introduction of 5nm/7nm

SAQP:

- Likely to be limited by power-performance impact due to dummies

EUV: HVM availability is the key

- Likely by the time it comes it would be in the 1D era

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CONCLUSION

Exciting time to work in design-technology co-optimization!

Need early study of the pros and cons of viable paths towards metal patterning (and other layers too)

- Silicon will speak louder than words!
- Expect more at next SPIE and other conferences

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