Design For E-Beam Using Talus on a 65nm Test Chip

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FASTRACK DESIGN

Members of the eBeam Initiative

Santa Clara, CA | April 2, 2009

D2S, Inc. and the eBeam Initiative

- Founded March, 2007
- Headquartered in San Jose, CA
- Dev. office in Shin-Yokohama, Japan
- Round A in 2007, led by Benchmark
- Completed Round B in March, 2009

- 10/08 : D2S-Fujitsu/e-Shuttle collaboration
- 01/09 : D2S-Vistec/ST/CEA/Leti collaboration
- 02/09 : eBeam Initiative launched with 20 companies including D2S and Fastrack (www.ebeam.org)

Fastrack

- **Fastrack Design is a *Premier Design Services* company.**
- **We strive to provide industry leading design solutions by staying in the bleeding edge technologies**
  - First tapeout in 2002
  - Implementation flow exclusively based on Magma tool suite
- **Our goal is to offer the best return on our customers' investments by providing unparalleled ASIC design services**

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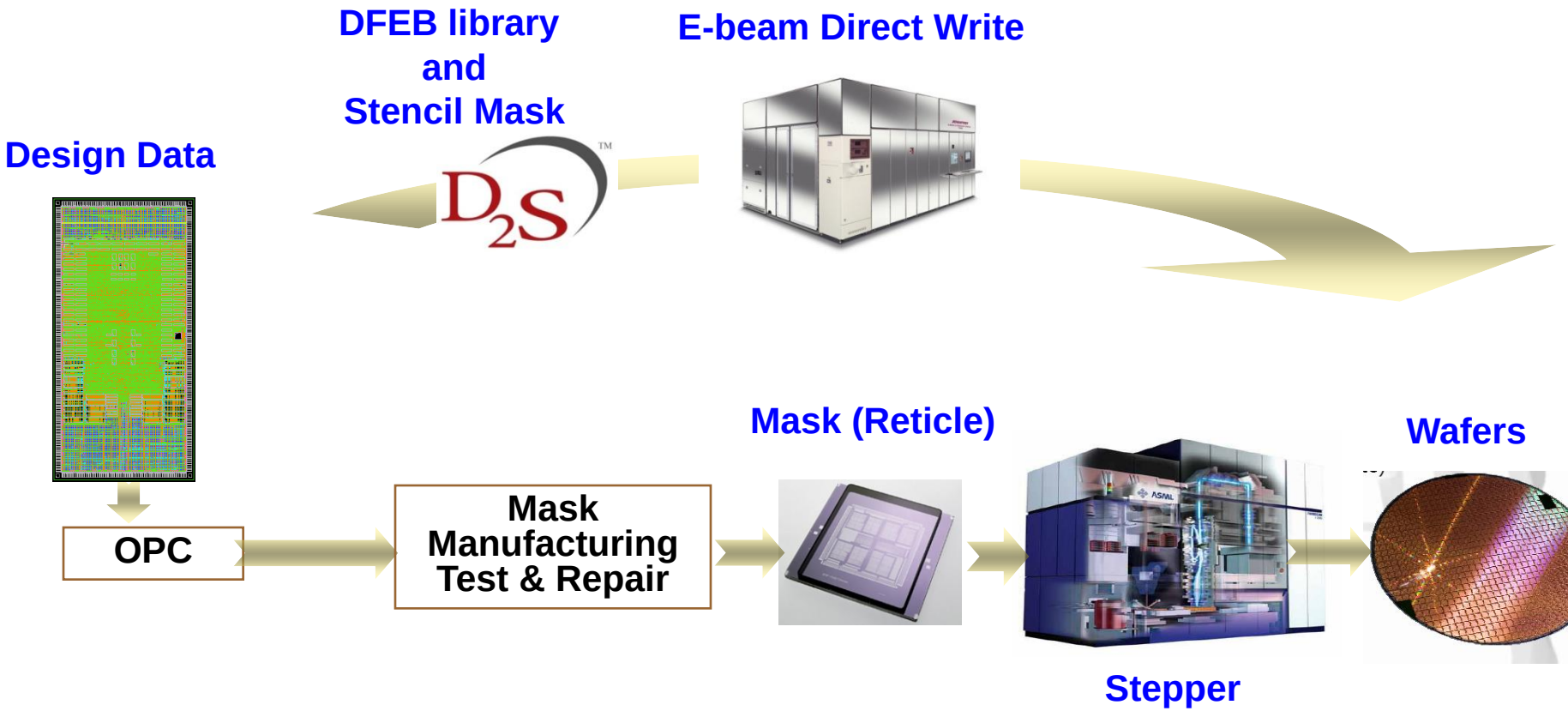
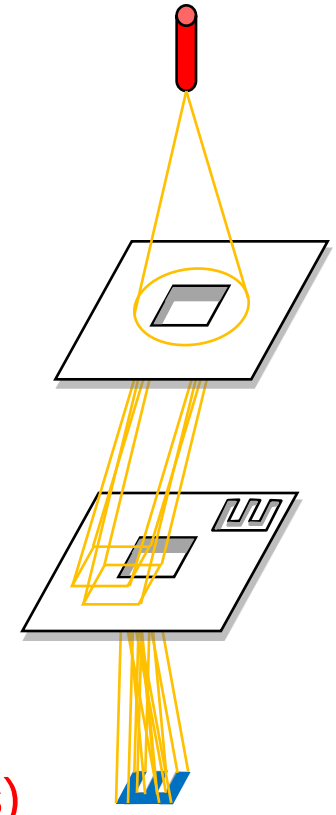
D2S FASTRACK DESIGN

DFEB enables Maskless All-Layer SoC Prototypes



CP shoots complex features in one shot

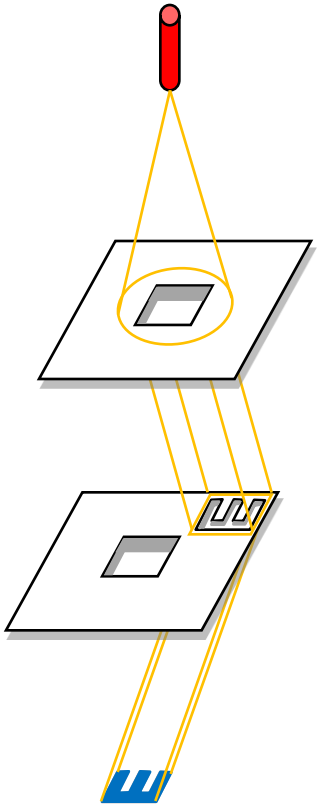


Electron Gun

1st Aperture

2st Aperture

Demagnification



Drawing courtesy of Hitachi High Technologies

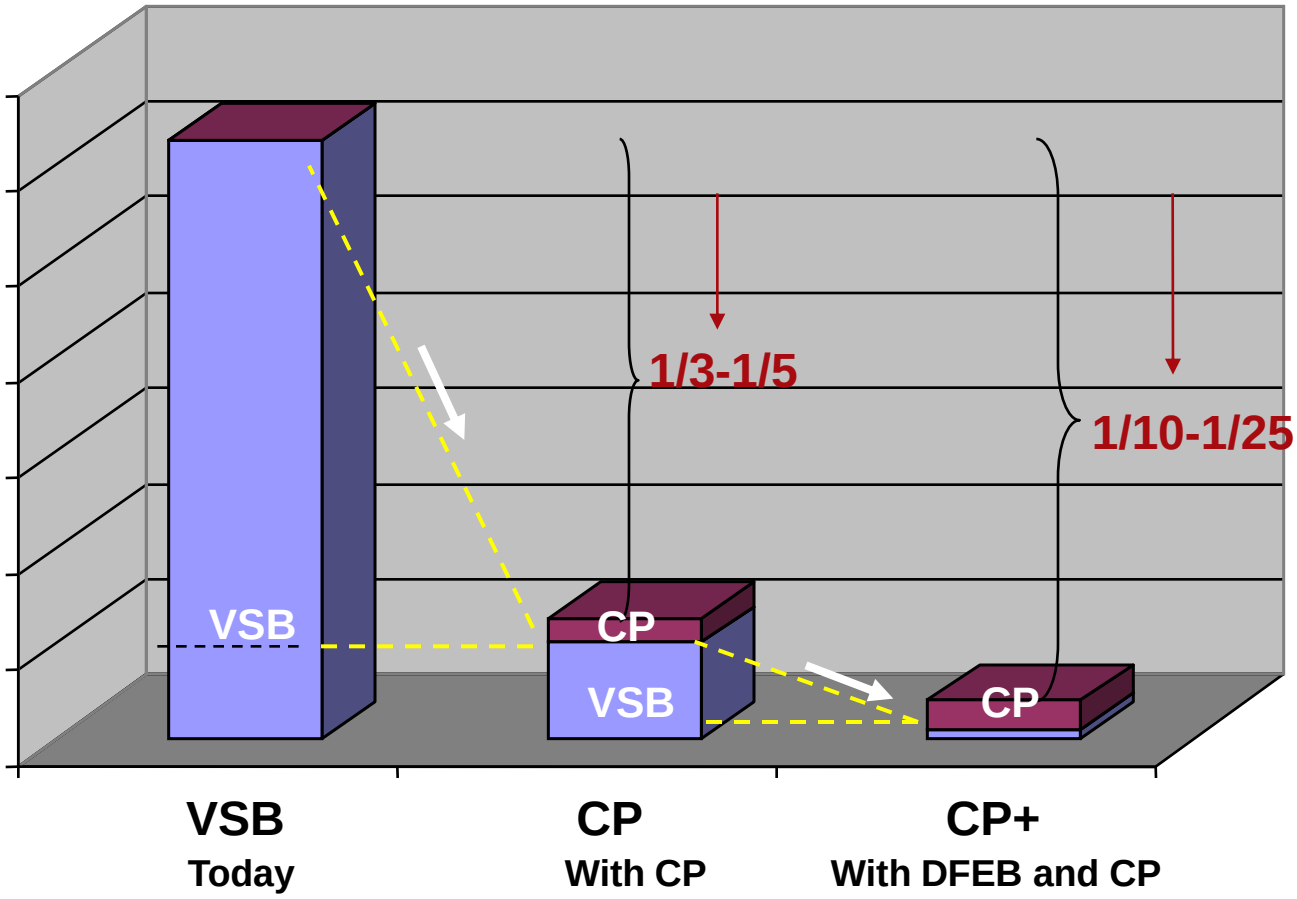
(4 shots)

(1 shot)

Variable Shape Beam (VSB)

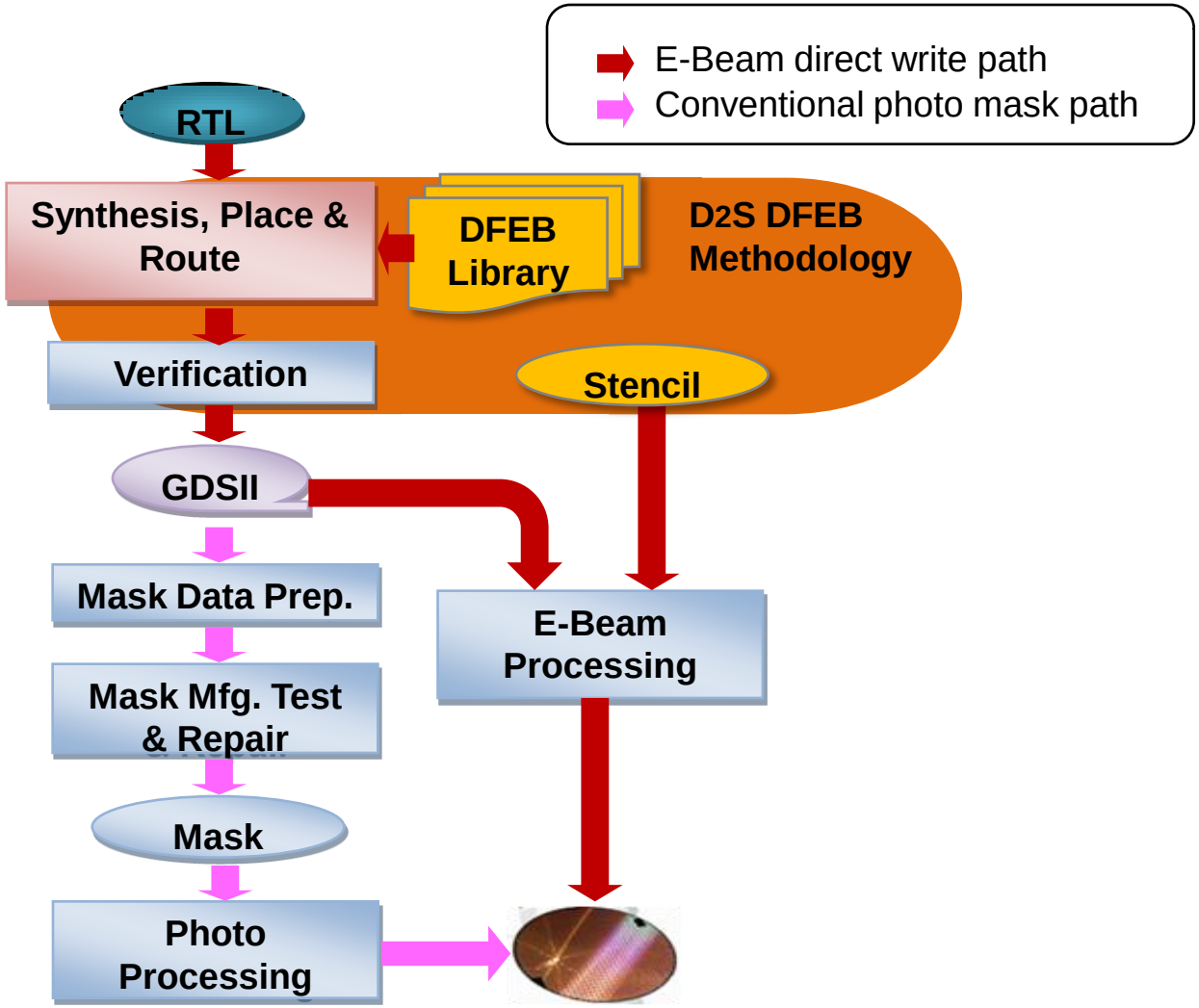
Character Projection (CP)

DFEB Decreases Required Shot Count

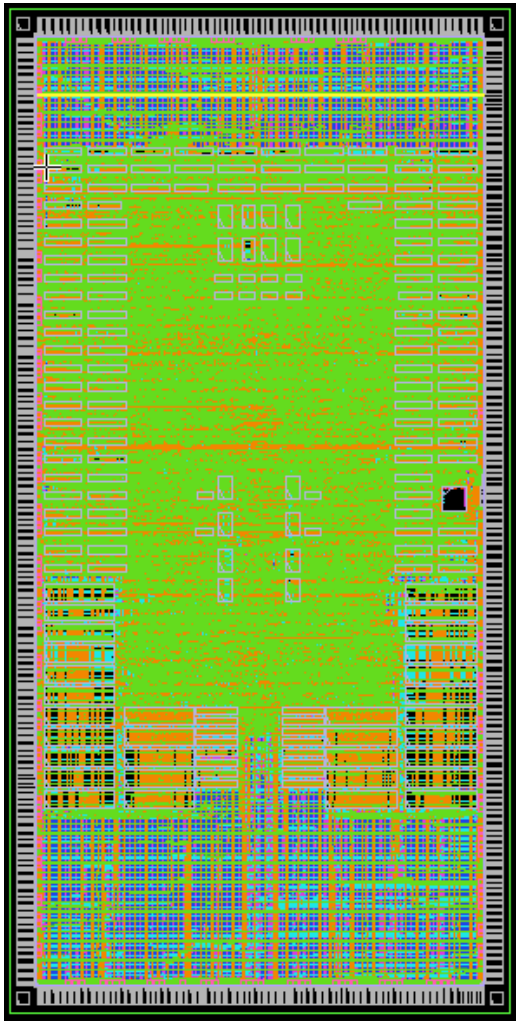


- **Makes EbDW practical for low volume prototypes**

DFEB Designs Can Also Be Made with Mask



65-nm Test Chip



- Target for 65-nm low-power, 7-metal layers process
- Approximately 3+ Million gates
- Chip size is 4.2 X 8.4 mm2
- Voltages are 1.2V for core, and 3.3V for IO
- Clock frequencies are 166Mhz and 162Mhz
- Designed using DFEB library as much as possible
- Shot count reduction of 10X

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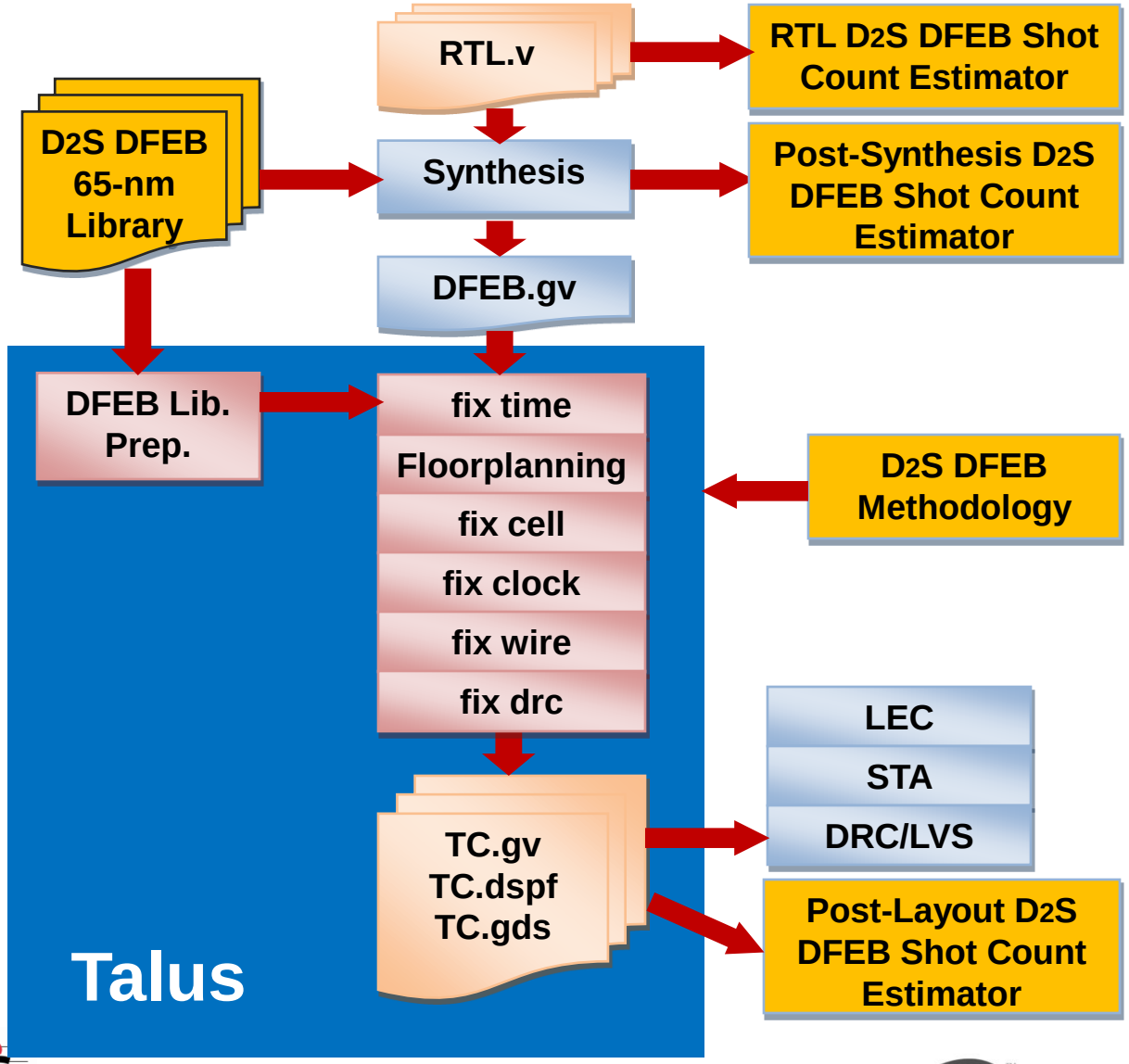
D2S FASTRACK DESIGN

Test Chip DFEB flow overview



DFEB Methodology Considerations for Talus

- **Implement using DFEB cells to maximize for shot count reduction**
  - 158 DFEB overlay cells are built from existing standard cells library
    - Strongly prefers north/flip-south orientations
  - DFEB cells Include memory cells for maximizing memory macros shot count reduction
    - Memory macros strongly prefers north/south orientations
- **Force "hide" the conventional standard cells initially, but re-introduce anytime in the flow to fix area, performance and power**
  - DFEB and conventional standard cells orientations can be relaxed also
- **Optimizing for shot count reduction with DFEB cannot compromise the quality of results**

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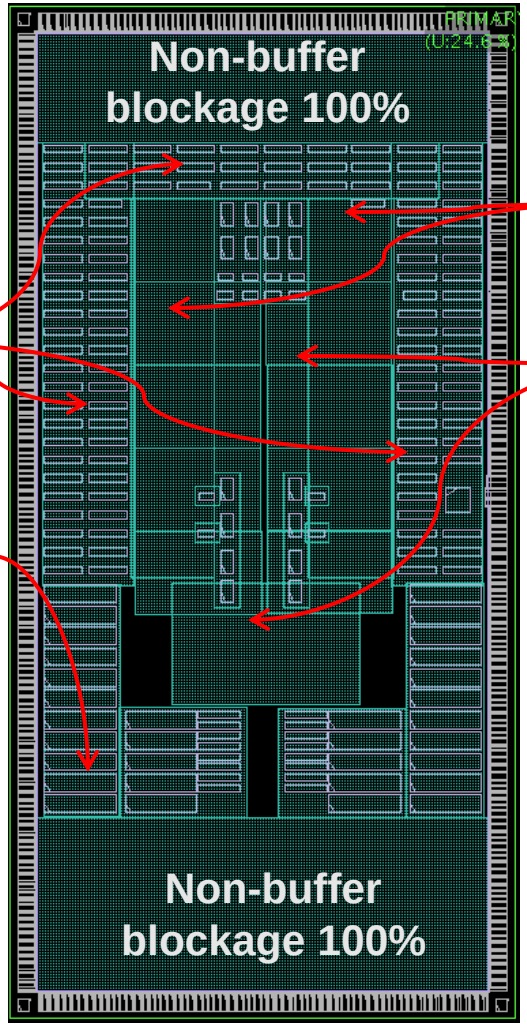
D2S FASTRACK DESIGN

Talus with DFEB was very easy

- **Default Talus flow scripts efficiently handled DFEB methodology**
- **No custom modifications were required, except for floorplanning and power planning**
  - It is the same with any SoC design

Floorplan: Test Chip

Fixed footprint of 4.2 X 8.4 mm²



Non-buffer blockage 100%

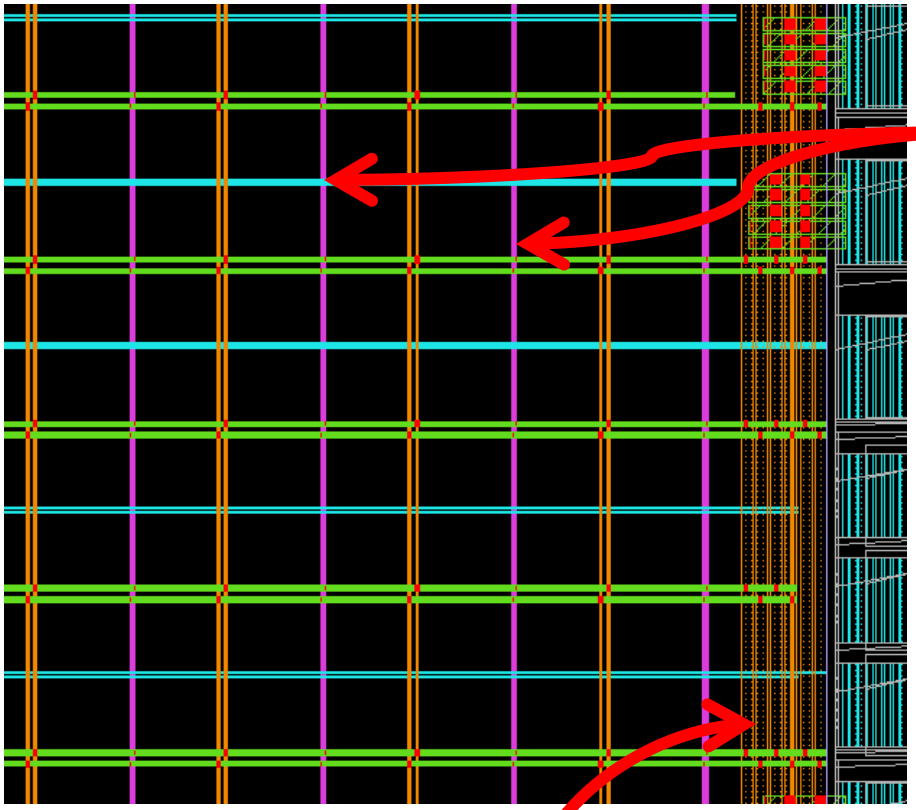
Non-buffer blockage 35%

Non-buffer blockage 10%

Use non-buffer blockage to:

1) **Relieve congestions**
2) **Tighten utilization**
   a) **Reduced cell area**
   b) **Shorten wire lengths**
   c) **Easier timing closure**

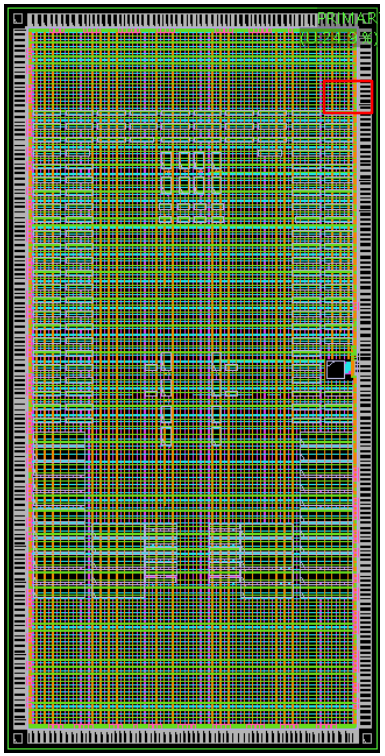
Power Planning: Meshes and Chip View



Power/Ground mesh are spaced between 400-500 tracks

Mesh view

Power/Ground rings are wider
Metal widths are integer multiple of 1um



Full chip power plan

Timing Validation

Operating Mode	Input Timing				% diff
	Specification		Test Chip Achieved		
	min	max	min	Max	
PLL Active	3340ps	5340ps	3340ps	5177ps	0.0, 3.0
PLL Bypass	3340ps	5340ps	3340ps	5177ps	0.0, 3.0

Operating Mode	Output Timing				% diff
	Specification		Test Chip Achieved		
	min	max	min	max	
PLL Active	-470ps	-270ps	-494ps	-284ps	4.8, 4.9
PLL Bypass	-470ps	-270ps	-494ps	-284ps	4.8, 4.9

- In a single pass, Talus correlates very well with Third Party sign-off tools

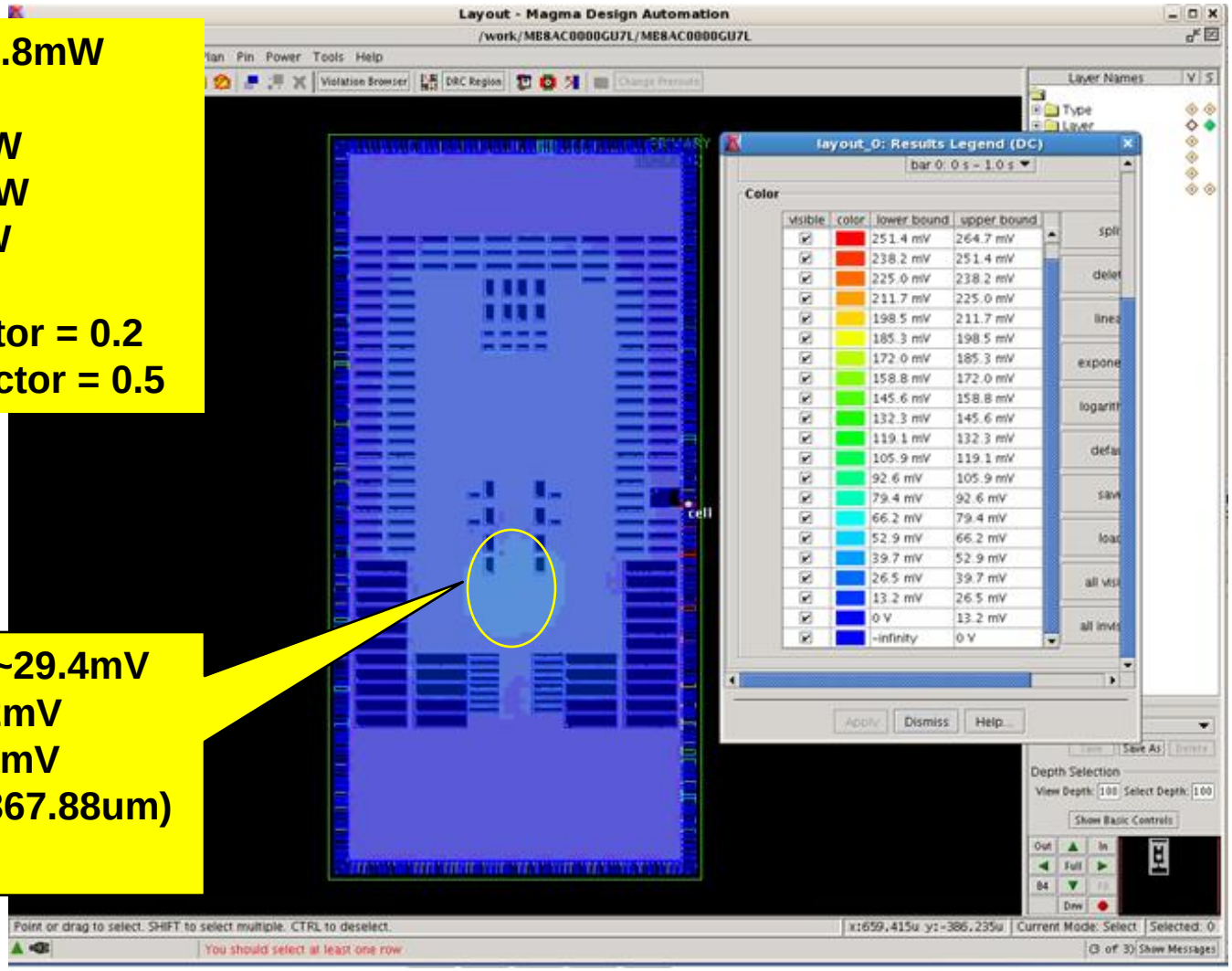
Power and IR Drop Met Requirements

Total power: 422.8mW

Leakage: 27.1mW
Internal: 132.6mW
Swcap: 263.1mW

Data activity factor = 0.2
Clock activity factor = 0.5

Max. IR drop: ~29.4mV
VDD: 15.2mV
VSS: 14.2mV
@(2043.6um, 3367.88um)



DFEB Shot Count Estimation

- **Shot count is added as an optimization criteria to area, performance, power, and yield**
- **D2S DFEB methodology optimize shot count through**
  - co-design of the cells and the stencil mask characters
  - synthesis, place and route flow
- **D2S DFEB Shot count estimation is available in every stage of the design**
  - Similar to timing analysis, there is successive refinement of the estimate
- **Cost of manufacturing with EbDW is directly related to shot count, even more than area**

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DFEB Test Chip Shot Count Estimation Report

Post-Synthesis D2S DFEB Shot Count Estimation			
	VSB Shot Count	DFEB Shot Count	Shot Count Reduction Ratio
Standard + Memories + IO + IP	315,709,961	36,320,156	8.69

Post-Layout D2S DFEB Shot Count Estimation			
	VSB Shot Count	DFEB Shot Count	Shot Count Reduction Ratio
Standard + Memories + IO + IP	312,856,334	29,572,509	10.58

- Shot count estimation at Post-synthesis stage provide more conservative reduction ratio
- Shot count estimation at Post-Layout stage provide more refined estimate
- Estimation is based on metal 1, contact, poly and diffusion

Talus Met Our Expectation

- No customization scripts required
- Met our area, performance, and power goal
- Single pass timing correlated well with third party tools
- Reduced turnaround time compared with Blast Fusion

Conclusions

- **DFEB with Talus is very easy**
- **Met our 10X shot count reduction goal**
  - Without compromising area, performance and power
- **Silicon validation is expected later in 2009**
- **DFEB enables maskless all layer SoC prototype**

Q&A

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