Design for E-Beam (DFEB)

A Novel Approach to EBDW Throughput Enhancement for Volume Production

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- EB friendly design
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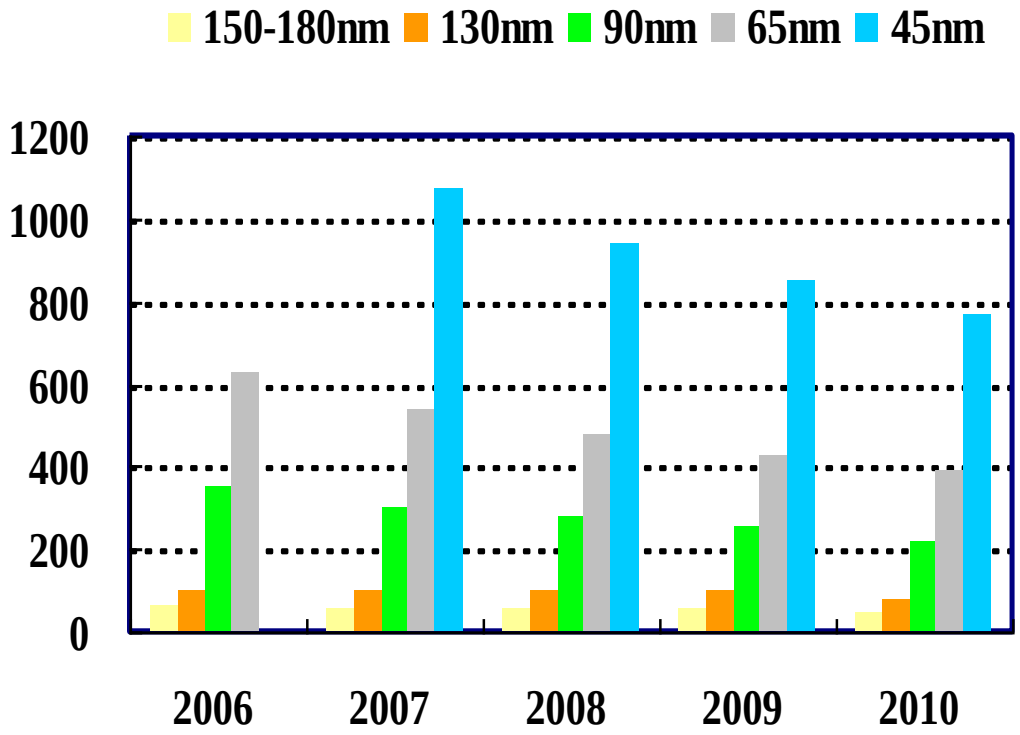
Takashi Maruyama, S. Sugatani, H. Tsuchikawa, *1H. Hoshino, *1Y. Machida, *1M. Ito, *2H. Tago, *3L. Chau, *3S. Lee, *4H. Komami

e-Shuttle, Inc., *1Fujitsu Microelectronics Limited, *2D2S KK, *3D2S Inc., *4ADVANTEST Corporation

Introduction

- Rising mask costs threaten the profitability of future custom LSI especially for 65nm node and beyond.



Reticle set price data

130nm reticule set price in 2006=100

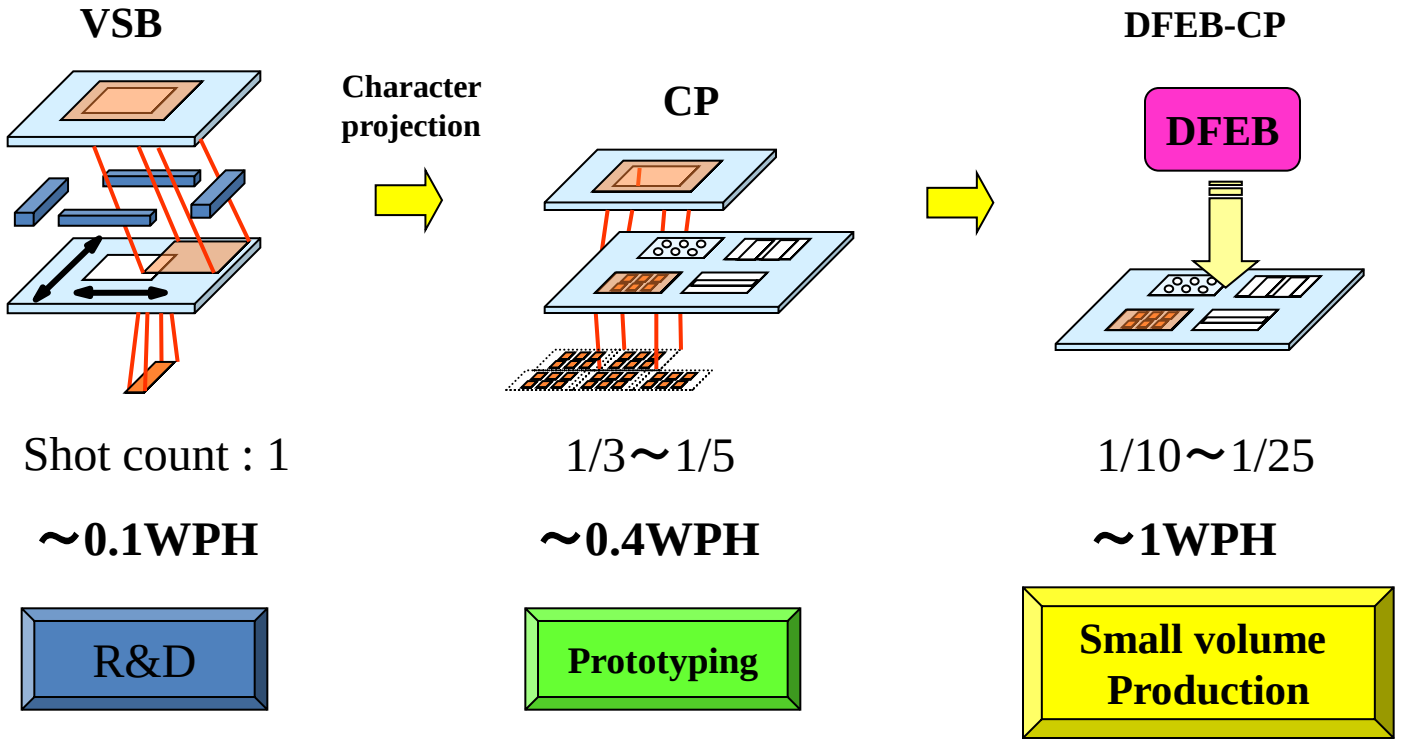
(Our identity)

Extend the business opportunities by providing less cost products with EB lithography

Motivation

Enhancement of throughput
to meet small volume production

- ✓ The ordinal shot count reduction with CP is by the recognition of repeatability
- ✓ Nevertheless the reduction efficiency is limited to around 4 times



DFEB (Design for Electron Beam)

➢EB friendly design layout data by tracing back to upstream design flow

DFEB Design Flow

CP friendly design

【Ordinal Lithography】

【DFEB】

Functional Design

Logic Design

Logic Synthesis

Layout Design

Product Data

Original Cell Library

DFEB Customization

Library Design

DFEB Cell Library Overlay

DFEB Stencil Mask Data

RTL

NETLIST

GDSII

Photo MASK Data

EB Exposure Data

DFEB NETLIST

DFEB GDSII

DFEB Exposure Data

(note)

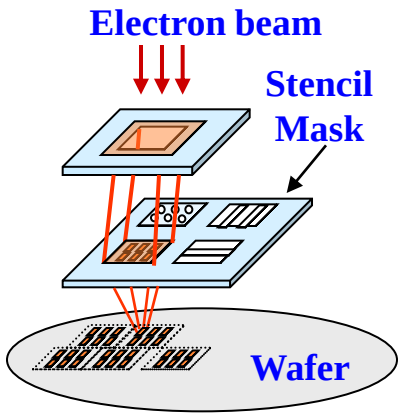
Photo

EB(CP)

EB(DFEB-CP)

DFEB Customization

- Cell selection
- Common base cell
- Partial CP conversion



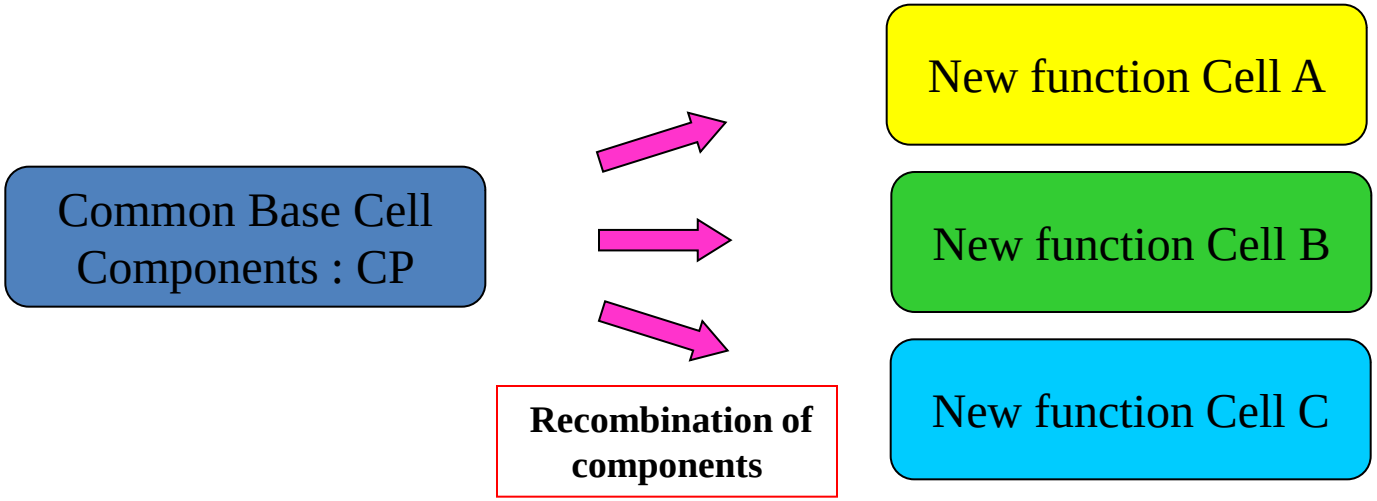
CP: Character Projection

(note) DFEB designs are compatible with mask-based volume production

DFEB Customization – Common Base Cell -

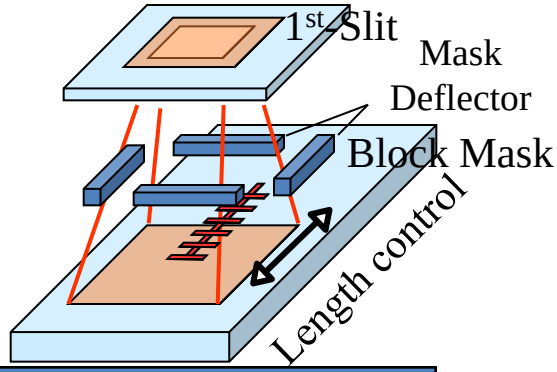
- Common component is a base structure to create new cell
- These components are put on the stencil mask as character
- With the recombination of these components, several new function cells can be created

More cell variations with less characters

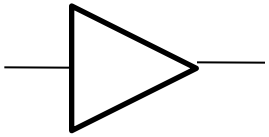
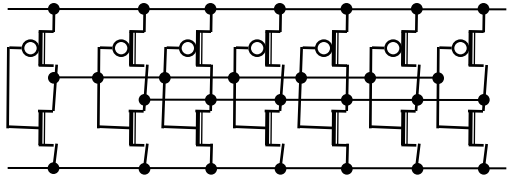
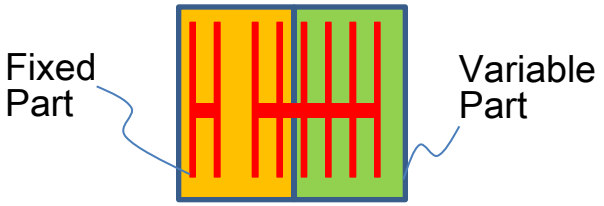
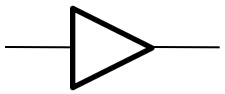
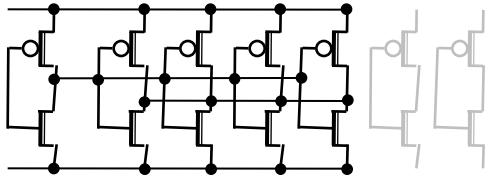
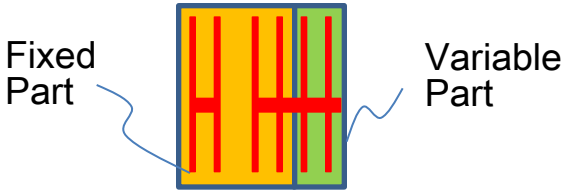
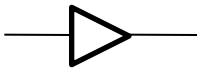
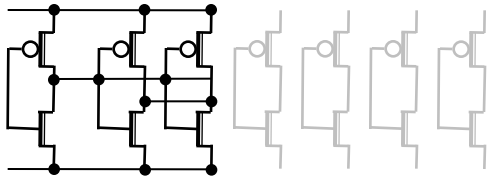
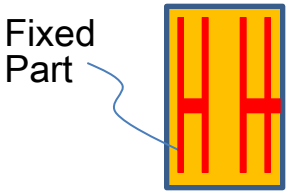


DFEB Cell Customization Using Partial CP Conversion

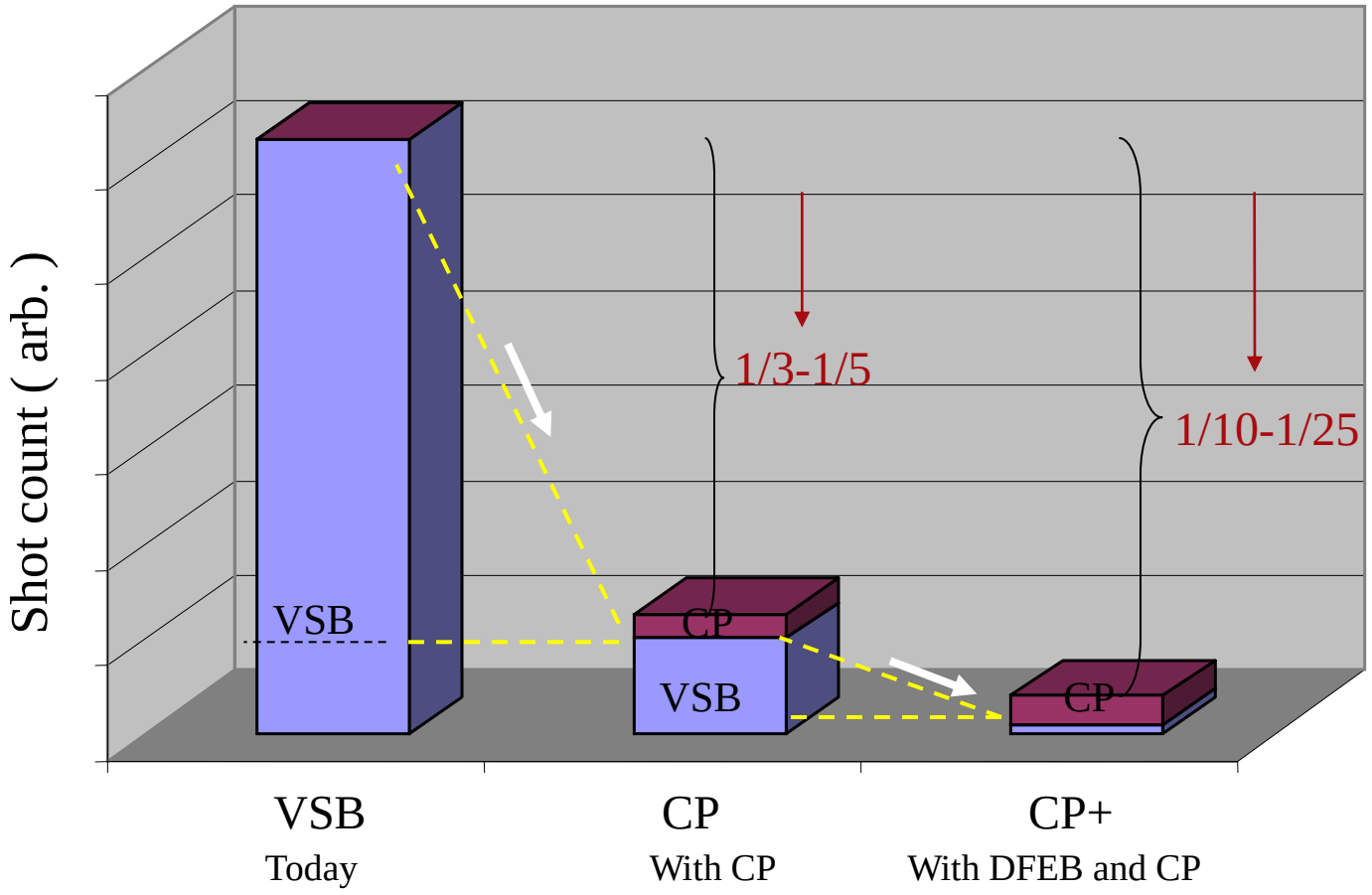
- A character for a large buffer is placed on a stencil.
- Middle buffer and smaller buffer image created using partial CP conversion.



Result: More cell variations with less characters.
One CP conversion is equivalent to about 9 ordinary characters.

Logic Symbol	Projected Circuit image on wafer	Partial CP Conversion
Large Buffer 		
Middle Buffer 		
Small Buffer 		

>10X Shot Count Reduction with DFEB

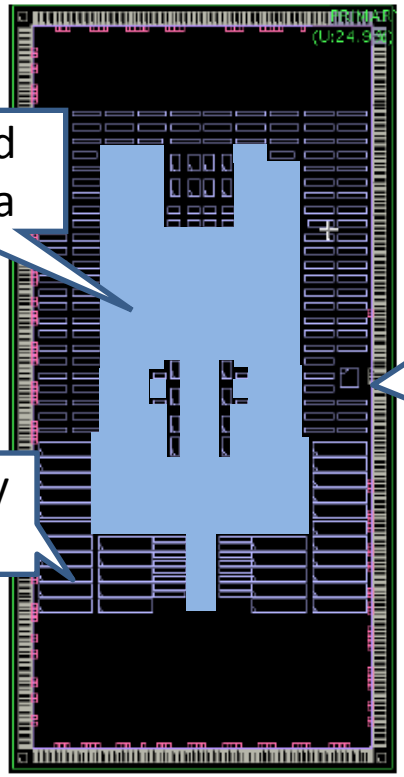


- Makes EBDW practical for low volume production

Test Chip Design Overview

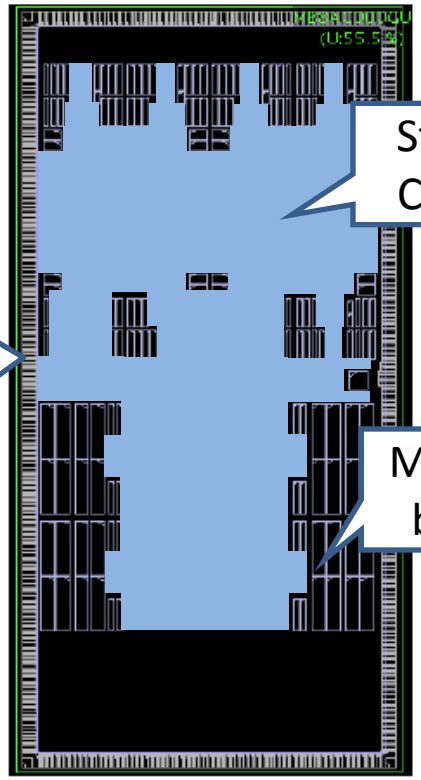
65nmLP

Chip-A floor plan with DFEB library
Chip size = 4.2mm*8.4mm



1. Process: Fujitsu 65nm CMOS, 7 layer metal
2. Chip size: 4.2mm*8.4mm
3. VDD: 1.20v for core, 3.3v for IO
4. Clock: 166MHz, 162MHz and 33.3MHz
5. Random Logic size: 3+Mgates
6. Memory size: 786Kbit

Chip-B Floor plan with original library
Chip size = 4.2mm*8.4mm

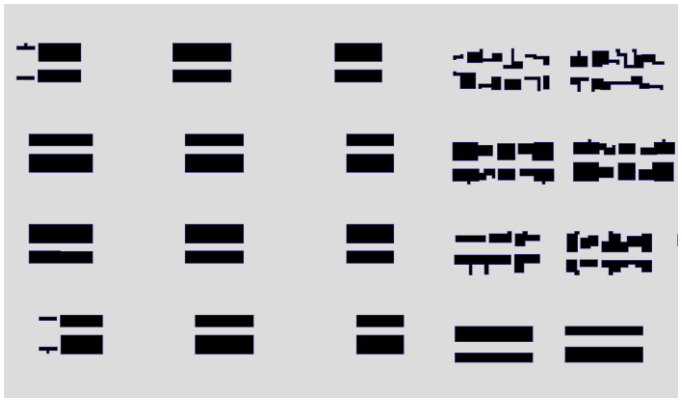


✓Test Chips were designed with both of DFEB library and Fujitsu original library

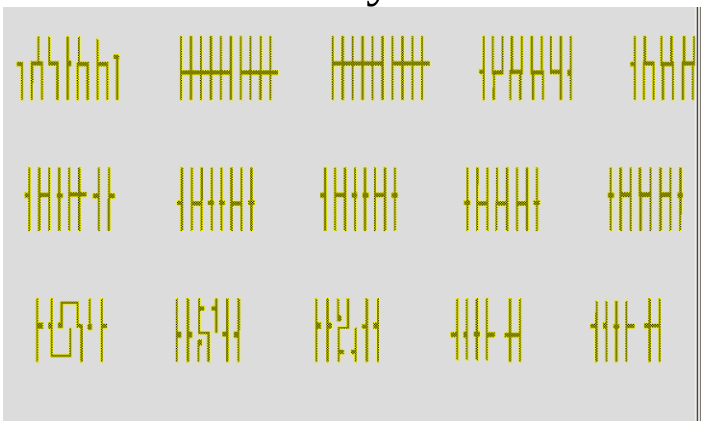
✓The practical Si was evaluated by function and power test

Character Layout for 65nm LP DFEB Design was Fixed

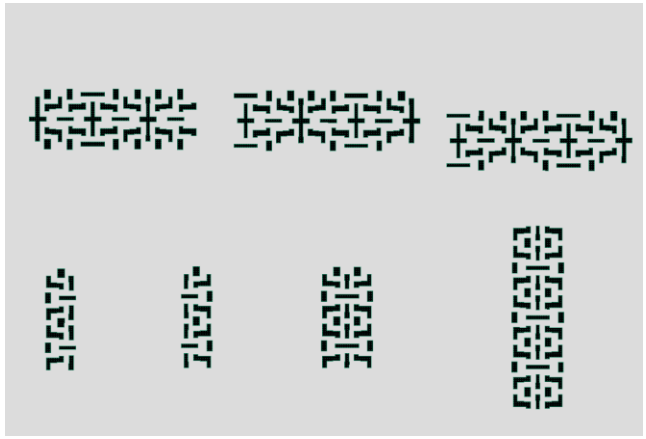
Diffusion (active)



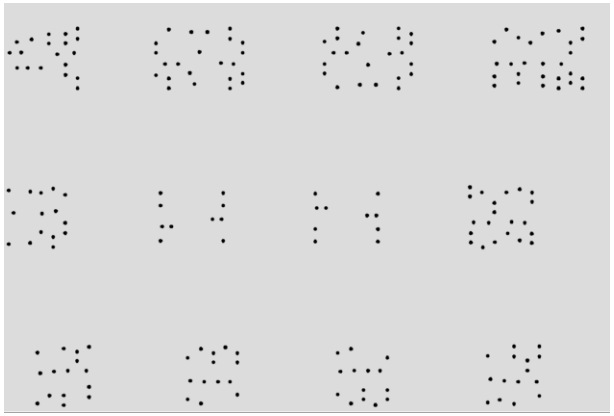
Poly



Metal-1

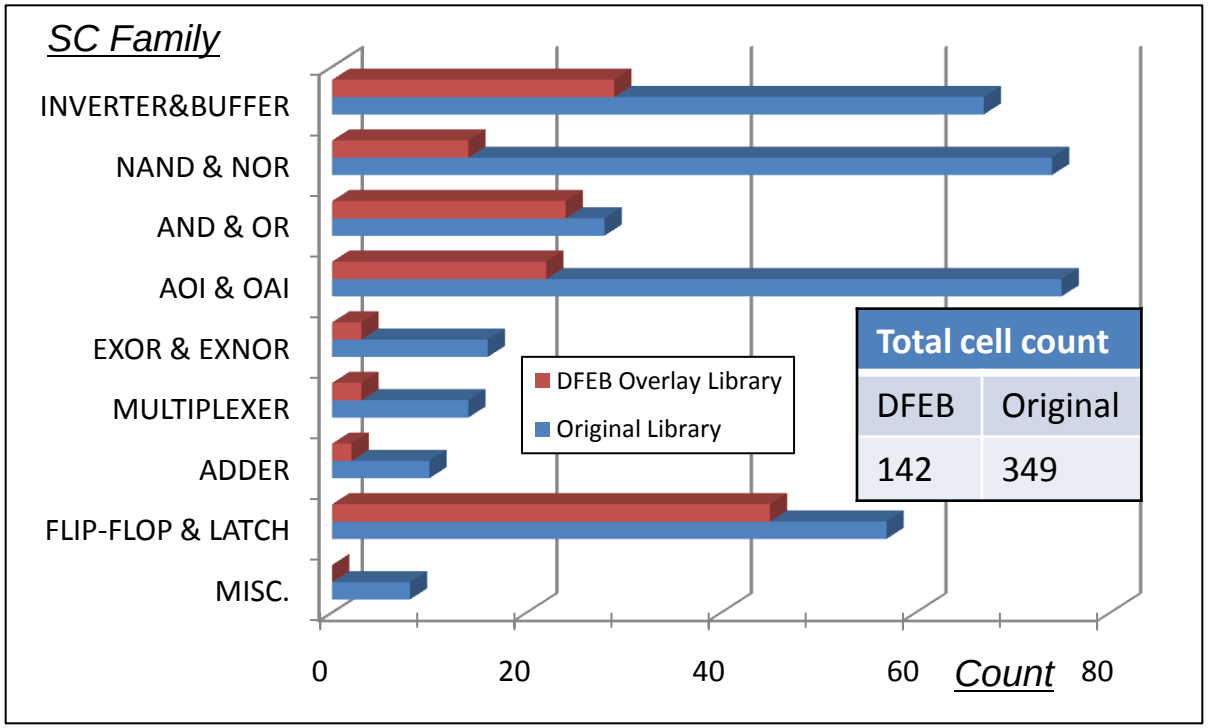


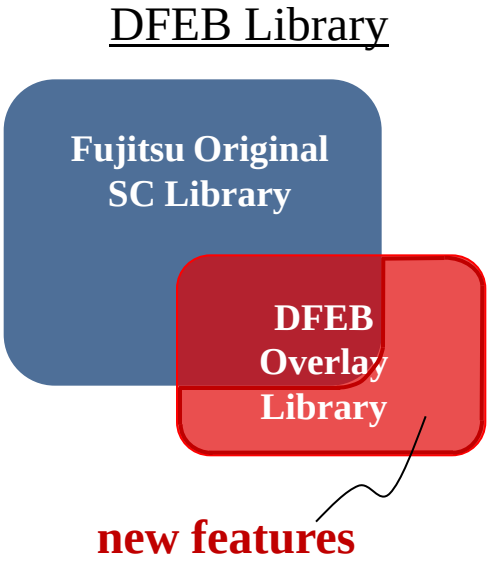
Contact



Test Chip Cell Library Usage

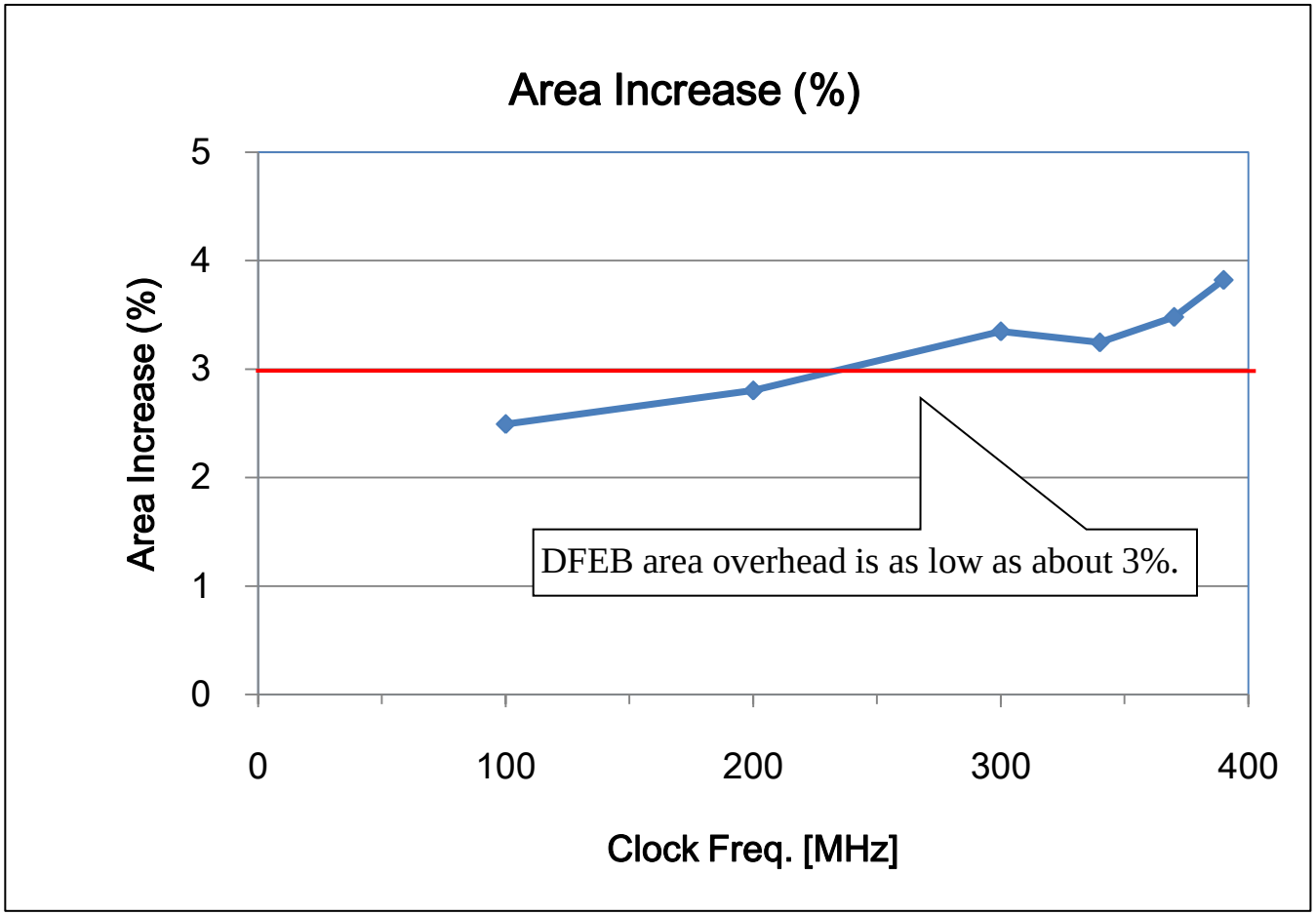
DFEB standard cell(SC) library is overlaid with the original library





- ✓ DFEB overlay library has a selected lineup in order to meet the number of character limits on a stencil mask.
- ✓ DFEB overlay library co-exists with the original library so that a designer can choose an original cell for better compatibility if necessary.

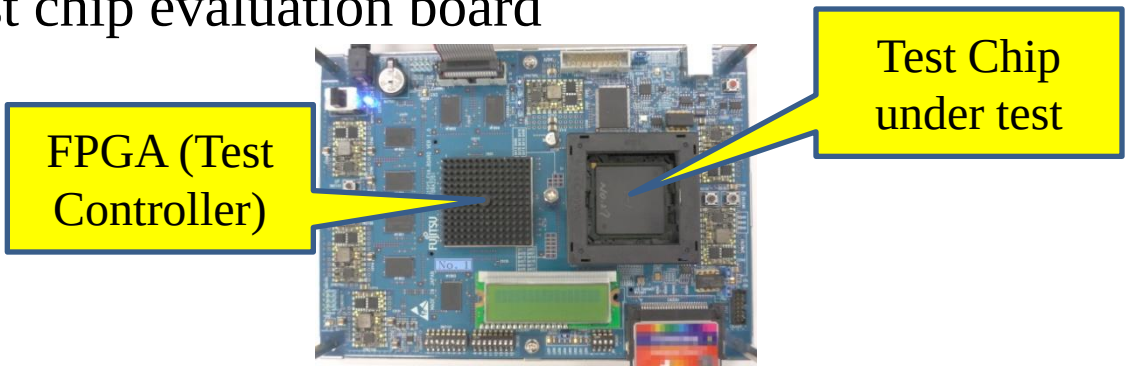
Test Chip Results Show Acceptable DFEB Area Increase



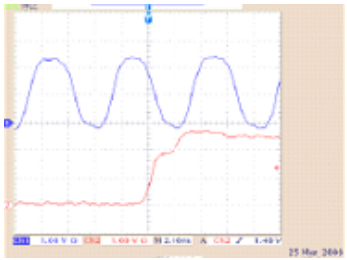
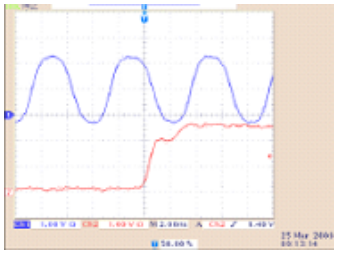
✓ Area increase at chip level is as low as 3% at 250MHz clock frequency point.
⇒We think it is permissibly low for practical use.

Test Chip Passes Function and Power Tests

- Test chip evaluation board



- Test chip evaluation results

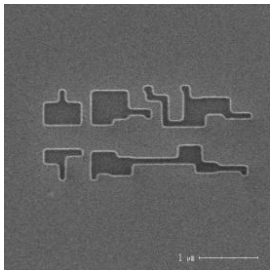
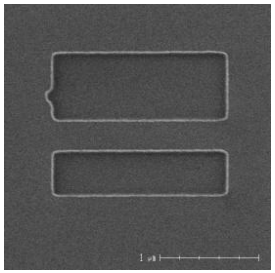
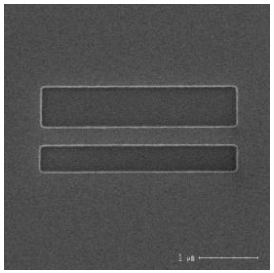
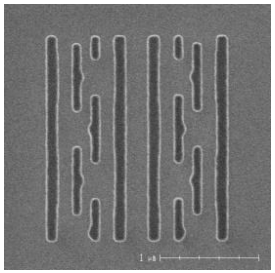
	Chip-A with DFEB library	Chip-B with original Fujitsu library
Signals	Clock signal An I/O signal 	
	No function difference between Chip-A and Chip-B is found.	
Measured Power Consumption (mW@166MHz)	112mW	111mW
	Measured power consumption numbers for Chip-A and Chip-B are very close.	

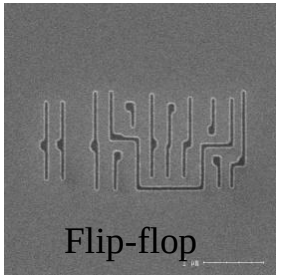
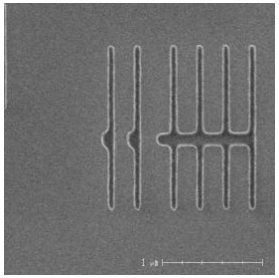
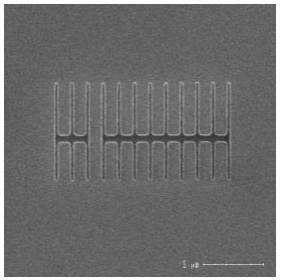
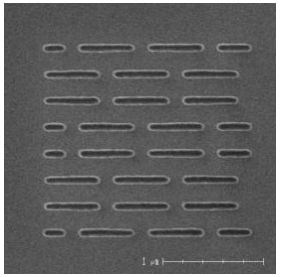
We have proved the DFEB design methodology available for production

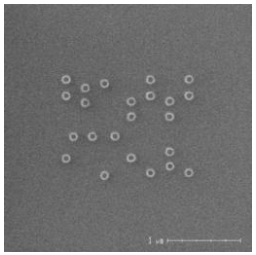
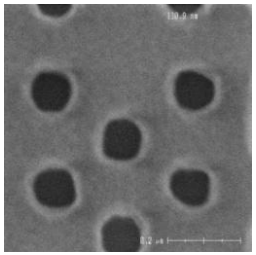
DFEB Character Exposure Results 1

✓All images are obtained by one CP shot which show good character count reduction

65nm LP



Active




Flip-flop

Gate

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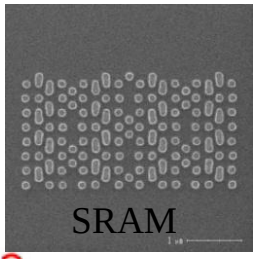
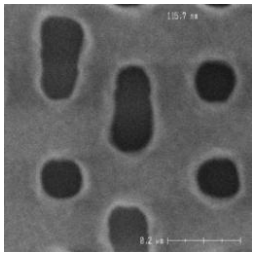
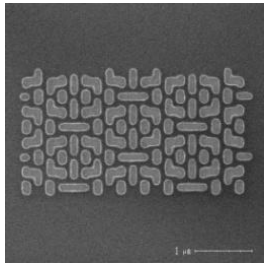
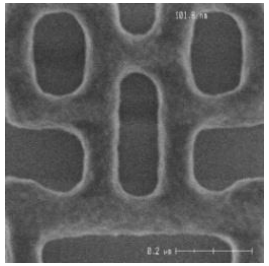
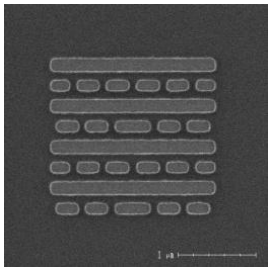
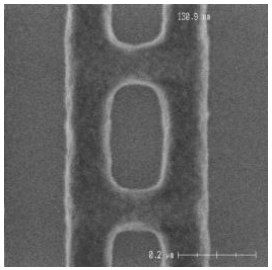
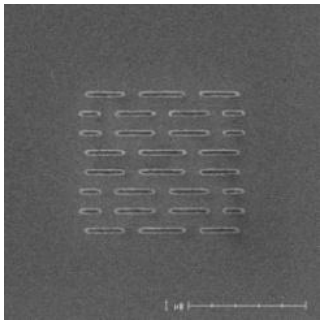
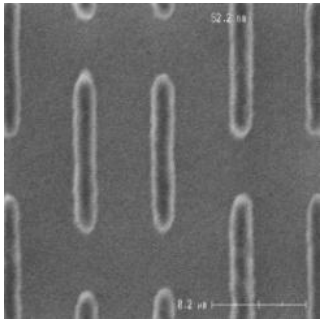

SRAM



Metal-1


Metal-2


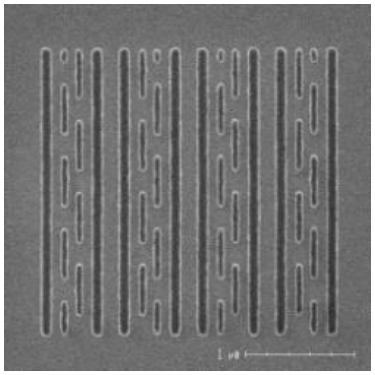
DFEB Character Exposure Results 2

✓All images are obtained by one CP shot which show good resolution





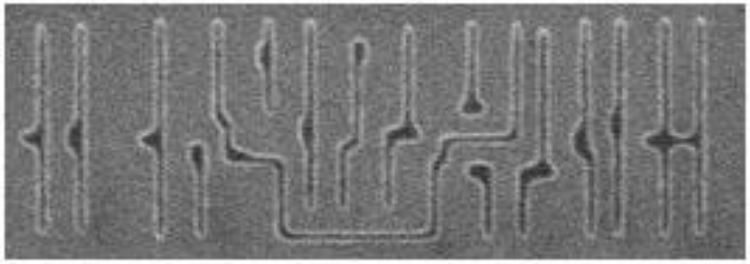
Active

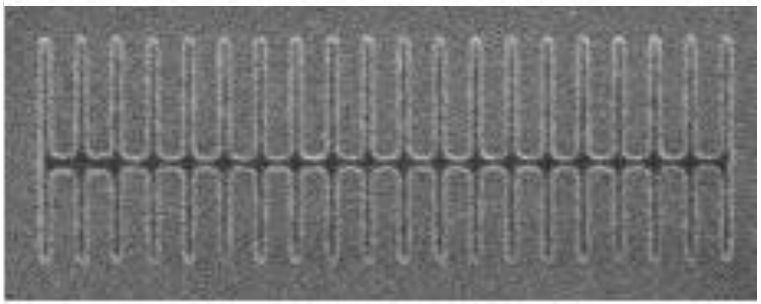


SRAM

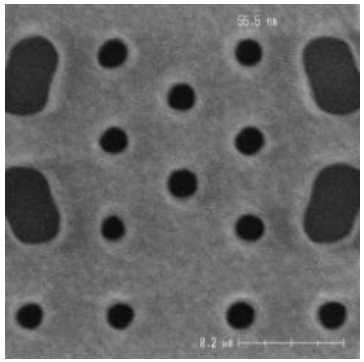
45nm node proto

Gate



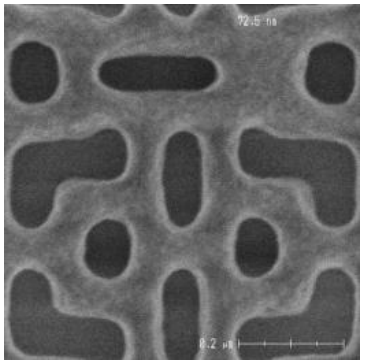


Contact



SRAM

Metal-1

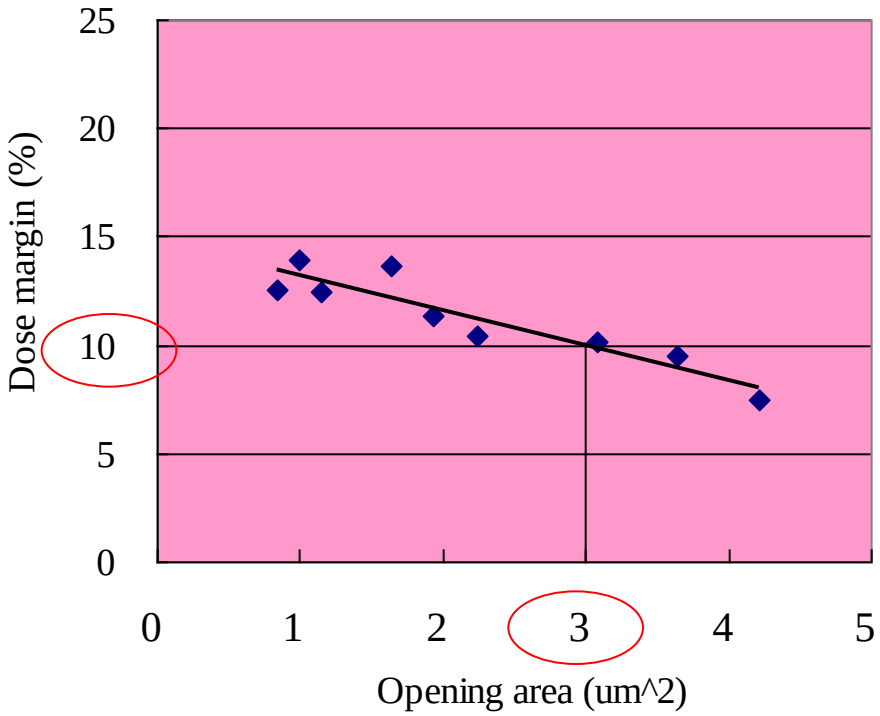


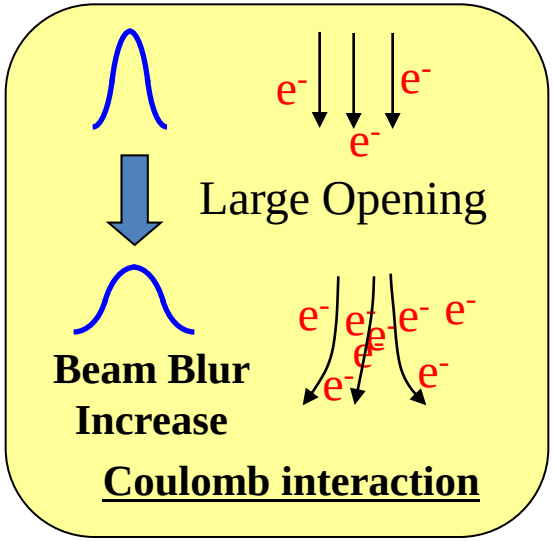
SRAM

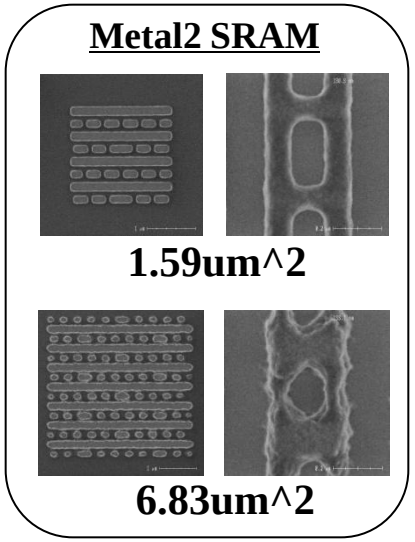
➢Enough potential in resolution

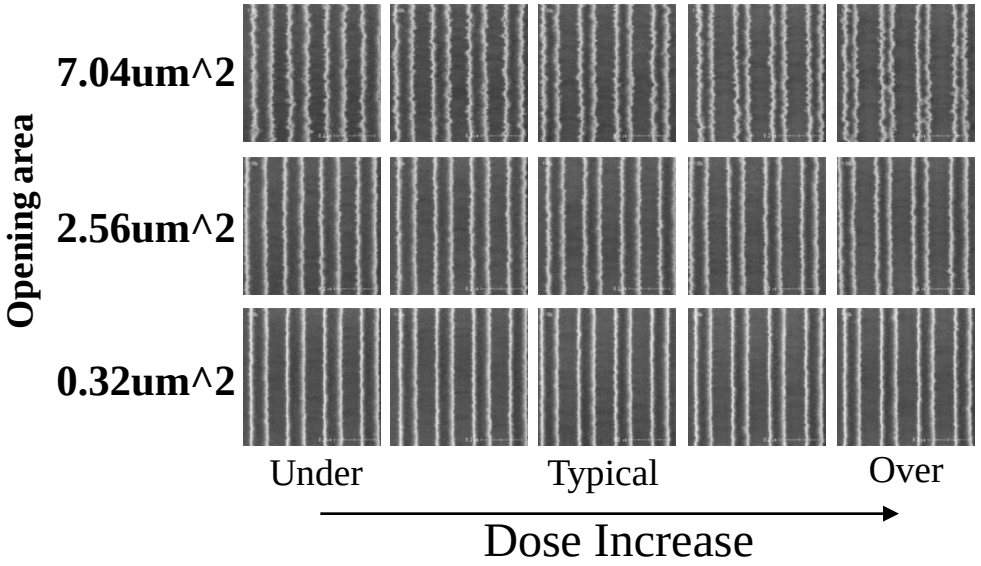
Coulomb Interaction

Correlation between CD dose margin and opening area is estimated





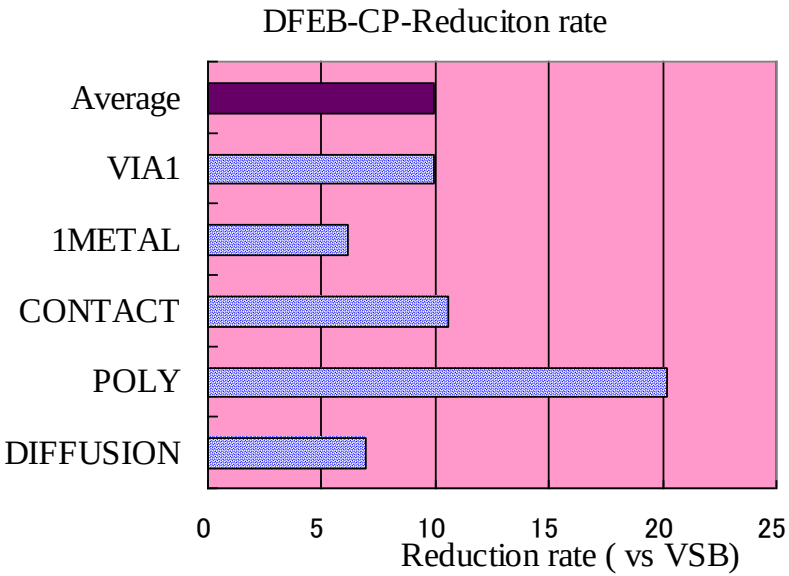


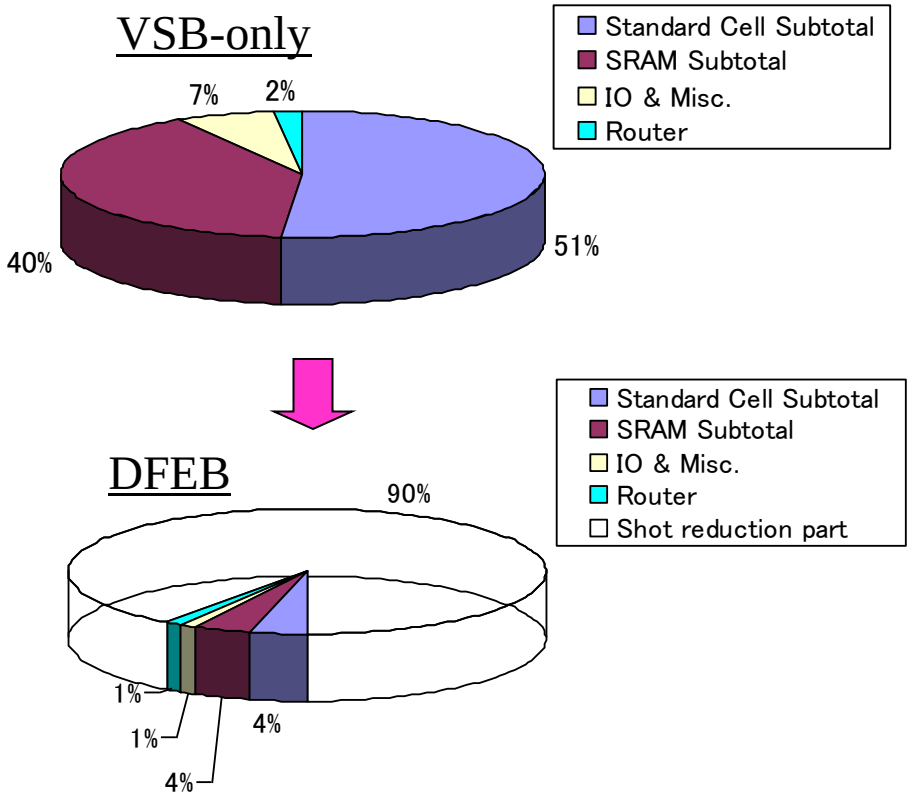


✓Available CP opening area is estimated from CD – DOSE data of 90nm L&S

10% dose-margin ⇒ 3um^2 Opening area

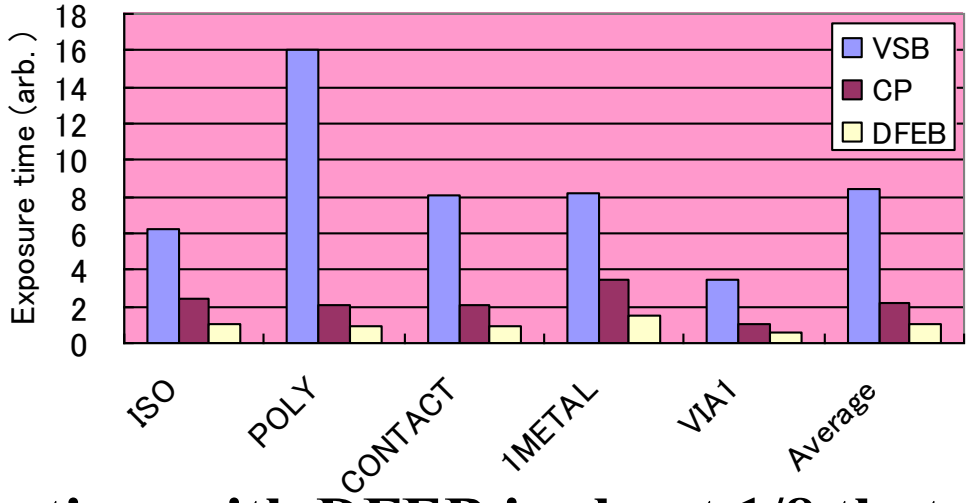
Shot Count Reduction with DFEB Validated （65nmTEST-CHIP）





- Shot count reduction rate with DFEB is about 10x that of VSB's
- Especially application to gate layer is effective at the value of 20x
- Shot count reduction efficiency is fairly well at standard cell part

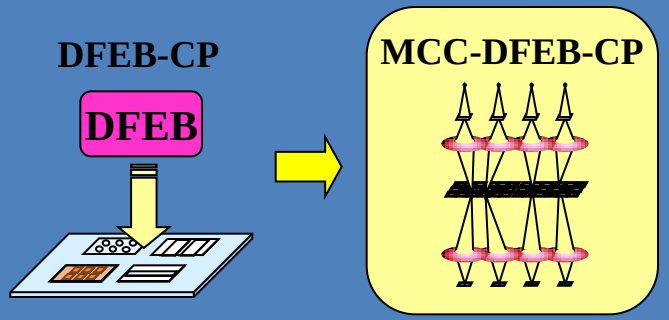
Exposure Time Estimation Results （65nmTEST-CHIP）



- Exposure time with DFEB is about 1/8 that of VSB's
- Especially application to gate layer is effective 1/16

[Future plan]

- DFEB combined with MCC
  - :Extension of available character number
  - :Multi-beam



	DFEB-CP	MCC-DFEB-CP
Shot count	1/10～1/25	1/100～
	～1WPH	**10WPH ～**

Conclusions

1. A 65nm test chip using DFEB design methodology was successfully designed, fabricated, and evaluated.
2. The test chip with DFEB shows identical function and runs at the same clock speed with the reference chip.
3. The CP exposure result with DFEB stencil shows good resolution performance to 45nm technology node.
4. Degradation of margin by coulomb interaction was estimated and available CP opening area was decided.
5. Shot count expectations were met and 10x was obtained for the test chip for diffusion, gate, contact, and Metal1 layers.

We have proved the DFEB available for small volume production

Takashi Maruyama e-Shuttle Inc.
E-mail : marutaka@jp.fujitsu.com

Thank you !

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All the persons concerned
Fujitsu Microelectronics Limited, D2S KK, D2S Inc., ADVANTEST Corporation