



Introducing The eBeam Initiative

20 Charter Members & Advisors Across the Ecosystem

Jan Willis eBeam Initiative Facilitator



Why Industry Collaboration?



- Removes barriers to adoption of design for e-beam (DFEB)
- Increases investment in multiple supply chains
- Inspires leadership

More designs, Faster Time to Market



eBeam Initiative Roadmap



Initiative Launch	Design Proven	DFEB Certification
>10 members, advisorsWebsite and papers	 65-nm test chip Methodology guide 45-nm test chip 	Design certification training

2008	2009	2010	2011	
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Semi-annual member meetings with advisors

Multiple Chip Suppliers		
 Design kit availability 		
 Equipment readiness 		







Industry Need for DFEB

Aki Fujimura, CEO - D2S, Inc. Managing Sponsor – eBeam Initiative

Fujitsu Viewpoint

Shinichi Machida, President and CEO - Fujitsu Microelectronics America Steering Group – eBeam Initiative

eSilicon Viewpoint

Jack Harding, Chairman and CEO - eSilicon Corporation Design Team Advisor – eBeam Initiative

Summary and Q&A





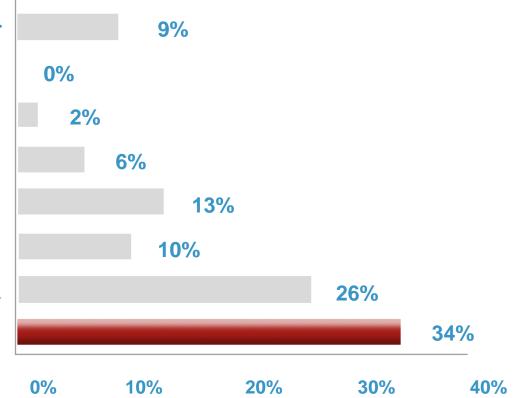
Industry Need for DFEB

Aki Fujimura CEO - D2S, Inc. Managing Sponsor - eBeam Initiative

Mask Cost is Top Concern

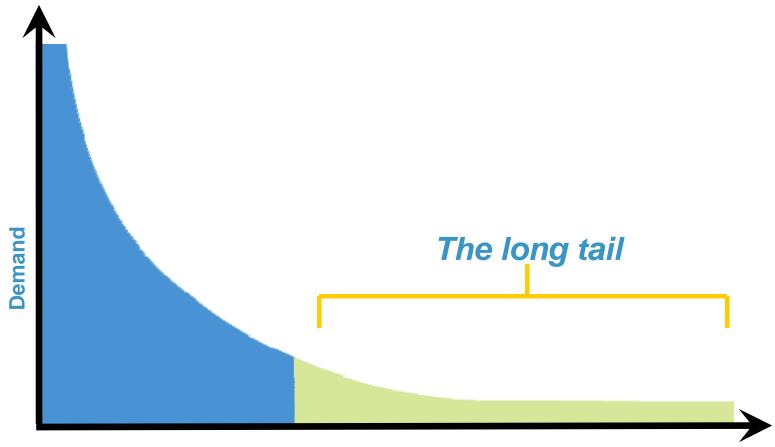


OtherTest costsPackaging costsSemiconductor IP qualitySemiconductor IP cost and...Inadequate EDA tools for...Increased design complexityHigher-mask costs



Source: Global Semiconductor Association (GSA) member survey, December 2007



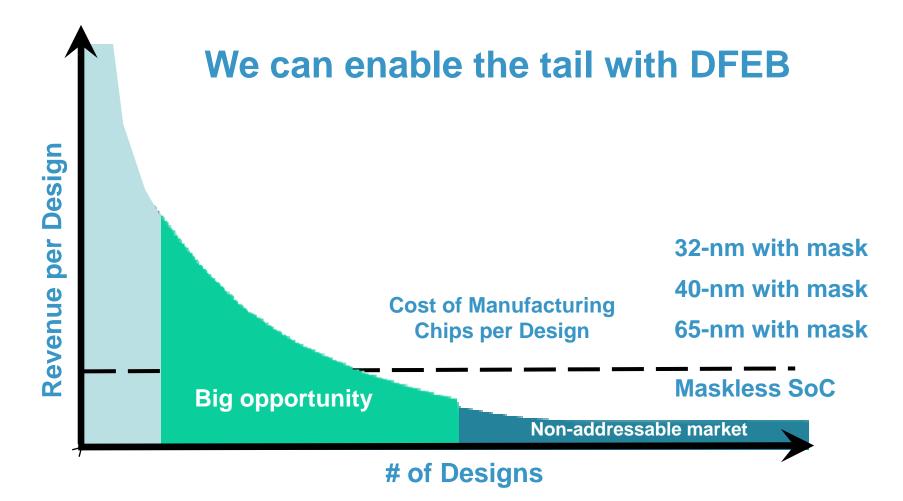


Popularity Rank

Source: Chris Anderson's "The long tail: Why the future of business is selling less of more"

The Tail is Getting Shorter



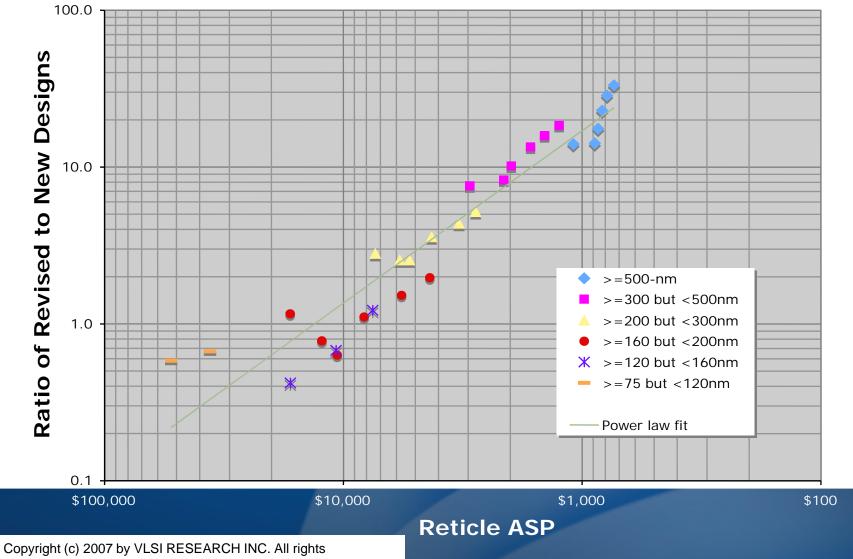




The Derivatives Opportunity



10x reduction in mask cost increases derivatives by 10x

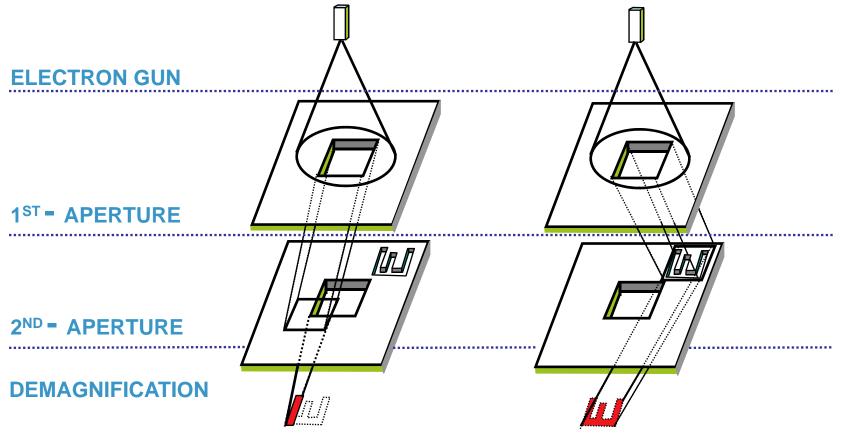


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Fast EbDW using CP



Available today and uniquely effective at and below 65-nm



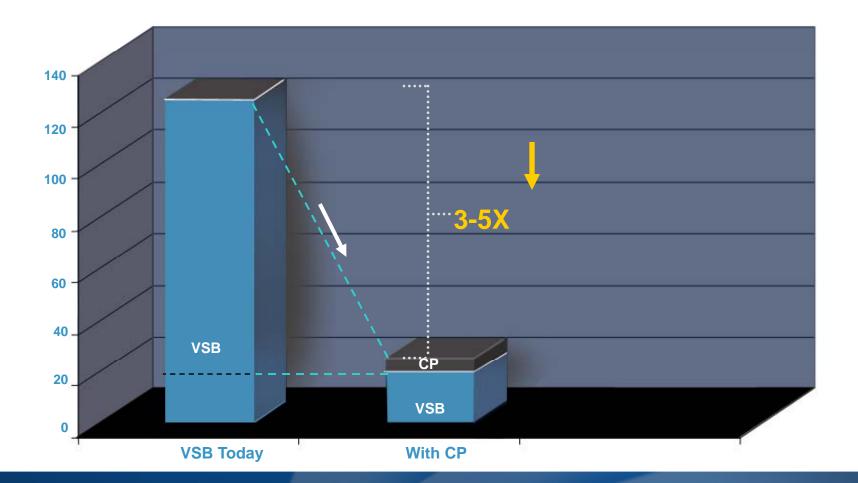
(A) VSB: Variable Shaped Beam

(B) CP: Character or Cell Projection

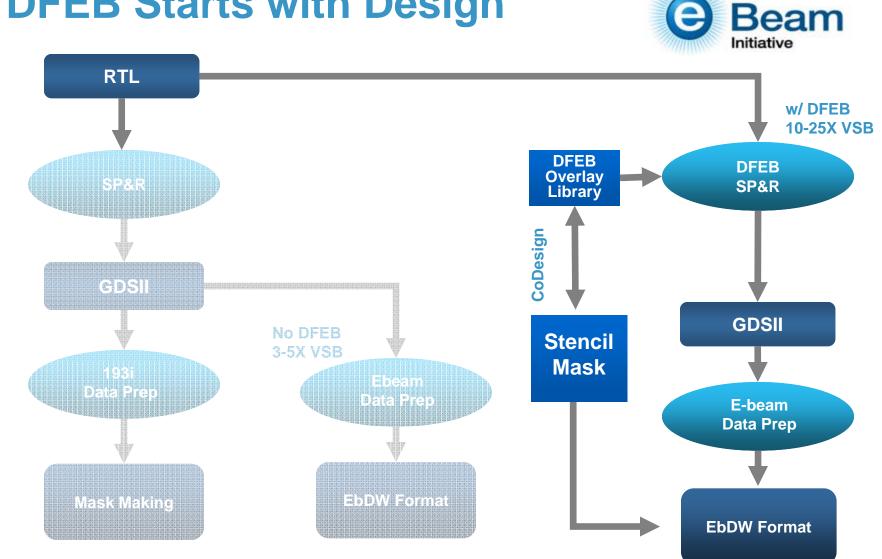
Drawing Courtesy Hitachi High-Technologies

EbDW Underutilized Even with CP due to throughput





Comparison Source: D2S Computer simulation of e-beam write time on a particular test case (speed up is dependent on aperture size and utilization %)

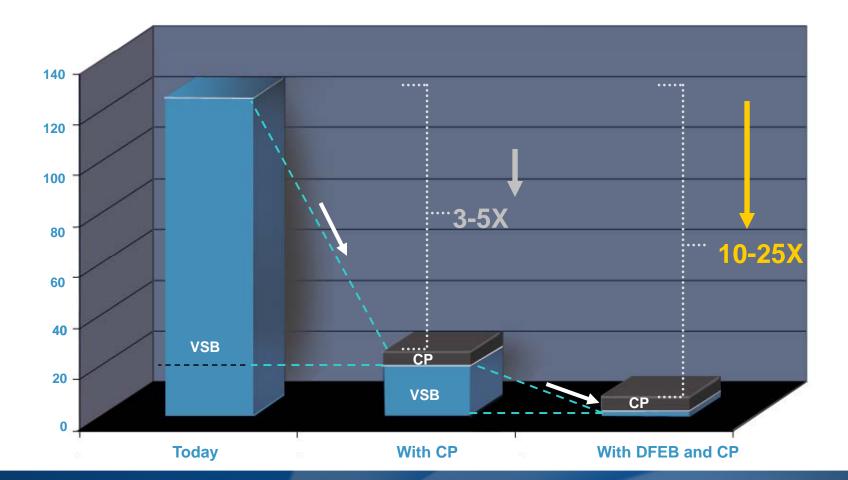


DFEB Starts with Design



DFEB Breakthrough Makes CP EbDW practical for low volume





Comparison Source: D2S Computer simulation of e-beam write time on a particular test case (speed up is dependent on aperture size and utilization %)

Collaboration Already Underway



- Fujitsu, e-Shuttle and D2S to Prove DFEB
 Design and Manufacturing
- 65-nm low-power test chip
- Announced October
 2008

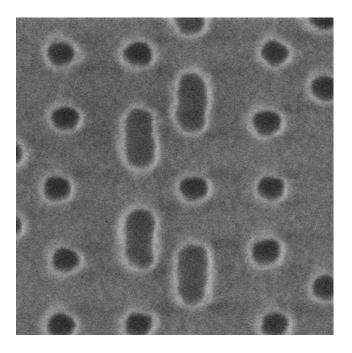
Pictured are (left to right) **Dr. Haruo Tsuchikawa**, President of e-Shuttle, **Hiroyuki Asahida**, Director of Marketing at Fujitsu Microelectronics, and **Aki Fujimura**, Chairman and CEO of D2S.



Today's Proof Point at SPIE



- CEA/Leti, Advantest, and D2S joint paper at 2:20 p.m., Session 5: EBDW
- Manufacturing proof of accurate CP projection for 32-nm contacts





Summary of Today's News



- 20 charter members launch the eBeam Initiative
- Initiative roadmap established
- Execution already underway
- Design test chip in 2009
- Today's SPIE paper proves manufacturability at 32-nm
- With DFEB, direct write has arrived





